Digital RF Control

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Outline

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- I-Q modulation/demodulation
  - in hardware
  - in software
- Microphonics compensation
- FPGAs

Motivation

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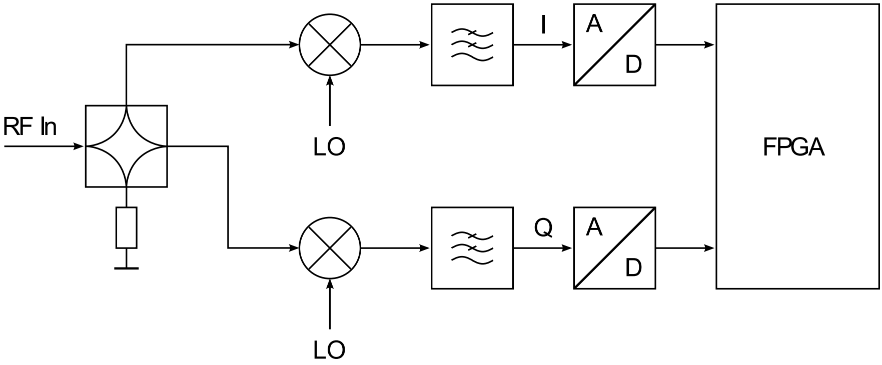
Why *digital* RF control?

- All controllers should be identical
- No offsets, no temperature drift, no noise,...
- Cheaper for accelerators with lots of cavities
- Upgradeable

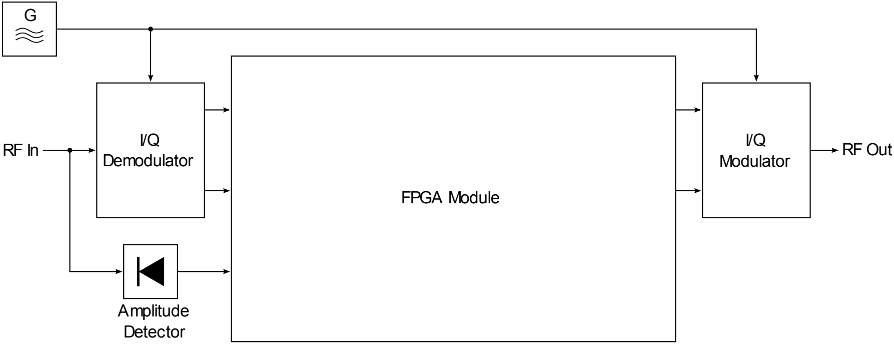
But

- Finite resolution of ADCs
- Latency

I-Q Demodulation in Hardware



I-Q Modulation/Demodulation in Hardware



I-Q Modulation/Demodulation in Hardware

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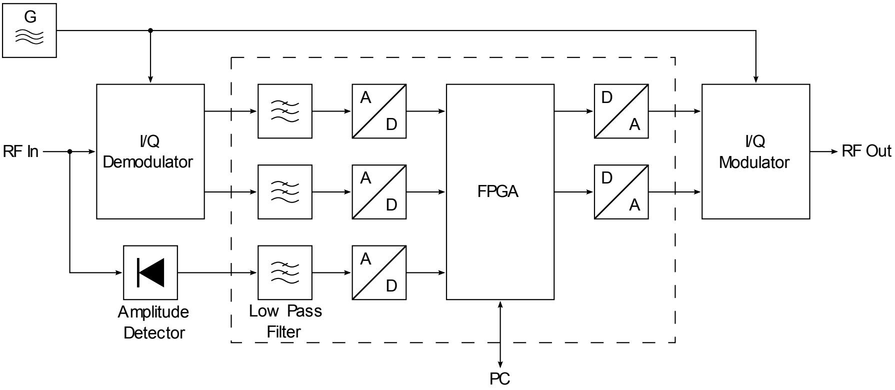

I-Q Modulation/Demodulation in Hardware

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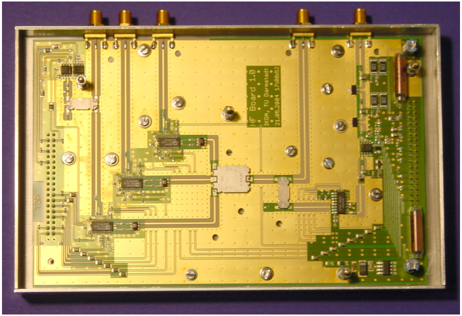

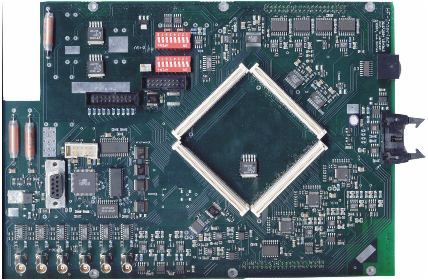

I-Q Demodulation in Software

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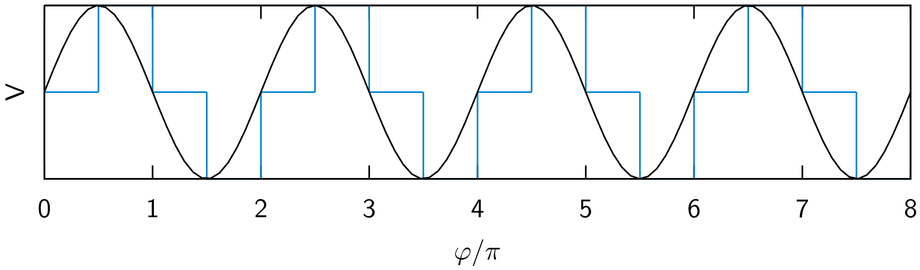
- Baseband: lots of offsets
- Idea: digitize at an intermediate frequency
- Sample signal in-phase and out of phase alternating
  e. g. $f_s = 4 \times f_{IF}$

I-Q Demodulation in Software



$$I = \quad V(0.5), -V(1.5), V(2.5), \ldots$$
$$Q = \quad V(1), -V(2), V(3), \ldots$$

I-Q Demodulation in Software

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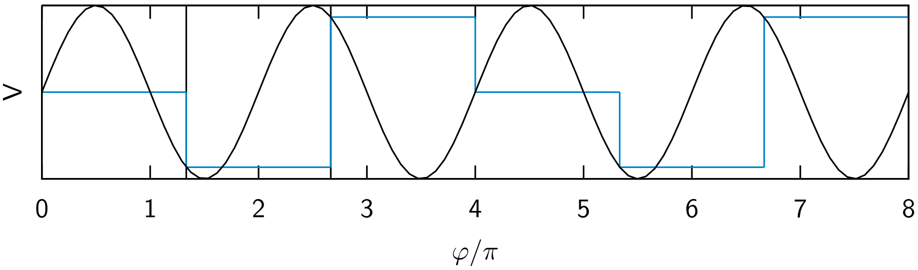

$$I_n = \frac{x_n \sin(\varphi+\Delta\varphi) - x_{n-1}\sin(\varphi)}{\sin(\Delta\varphi)}$$

$$Q_n = -\frac{x_n \cos(\varphi+\Delta\varphi) - x_{n-1}\cos(\varphi)}{\sin(\Delta\varphi)}$$

$$I = \frac{2}{N}\sum_{i=0}^{N-1} x_i \sin(\varphi + i\,\Delta\varphi)$$

$$Q = \frac{2}{N}\sum_{i=0}^{N-1} x_i \cos(\varphi + i\,\Delta\varphi)$$

Trigonometric functions can be precomputed

I-Q vs. A-φ control

I-Q control

+ Simple (two identical controllers)

A-φ control

+ Different amplification for amplitude and phase possible

Microphonics compensation

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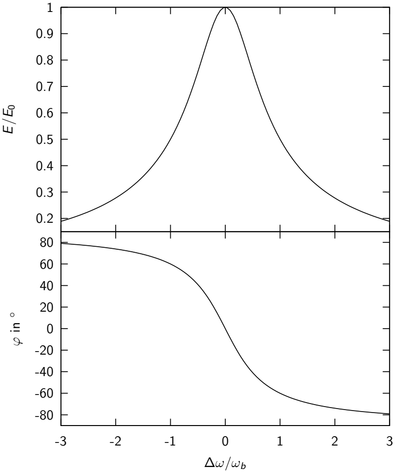

$$E(\omega) = \frac{E_0}{\sqrt{1+4Q_L^2\left(\frac{\omega-\omega_0}{\omega_0}\right)^2}}$$

$$\varphi(\omega) = \arctan\left(-2Q_L\frac{\omega-\omega_0}{\omega_0}\right)$$

$$E(\varphi) = \frac{E_0}{\sqrt{1+\tan^2\varphi}} = E_0\cos\varphi$$

$\Rightarrow$ raise power by factor $\frac{1}{\cos\varphi}$ to compensate for loss in magnitude caused by microphonics

Microphonics compensation

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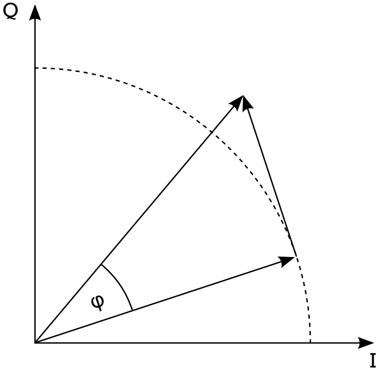

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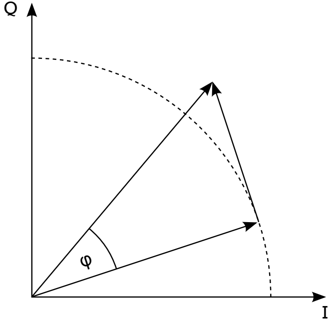

$$\begin{pmatrix} I' \\ Q' \end{pmatrix} = \left[\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} + p_{\mathrm{err}}\, k_p \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \right] \begin{pmatrix} I \\ Q \end{pmatrix}$$

Field-Programmable Gate Arrays (FPGAs)

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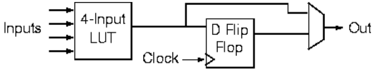
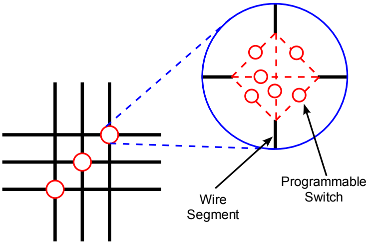
- Programmable logic device
- Consists of logic cells and wires

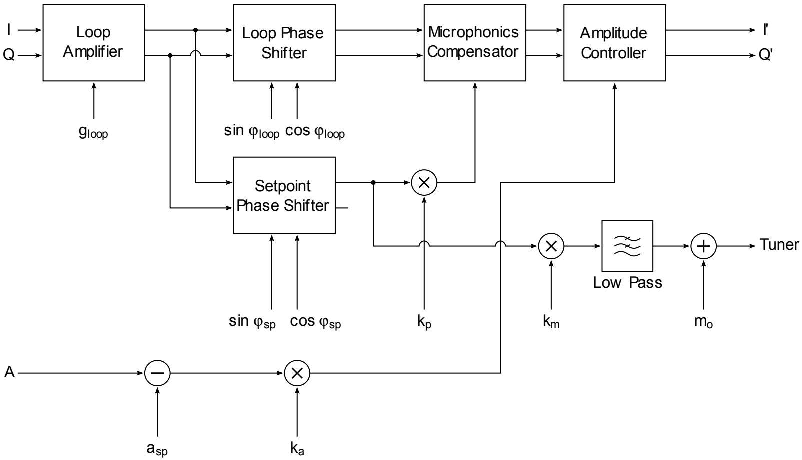




- Parallel processing is possible $\Rightarrow$ much faster than Microprocessors/DSPs
- Reprogrammable in circuit

Sketches: `http://en.wikipedia.org/wiki/Field-programmable_gate_array`

Control Algorithm for Self Excited Loop



Thank you for your attention

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