Pulsed Power Engineering
Advanced Topologies

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SLAC NATIONAL ACCELERATOR LABORATORY

Power Conversion
Solutions for Challenging Problems

Advanced Modulator Topologies

- Marx
  - Basic Marx
  - Solid state Marx
  - Inversion generator
  - Stacked Blumlein
  - PFN Marx
- Adder topologies
  - Inductive
  - Transmission line
- Resonant converter-modulator
- Magnetic pulse compression
  - Magnetic modulator
  - Branched magnetics
- Opening switch PFL

Basic Marx Generator

- Concept first proposed by E. Marx in 1925
  - Charge capacitors in parallel
    - Maximum voltage: V
    - Total capacitance: NC
  - Discharge them in series
    - Maximum voltage: NV
    - Total capacitance: C/N
- Applicable over wide range of parameters
  - Sub-μs < pulse length < multi-ms
  - ~0.1 MV < output voltage < over 10 MV
- Simplifies voltage insulation and reduces switch voltage by factor of N (up to ~100)
  - Relatively low voltage on long time scales (charging)
  - High voltage only present while being delivered to load

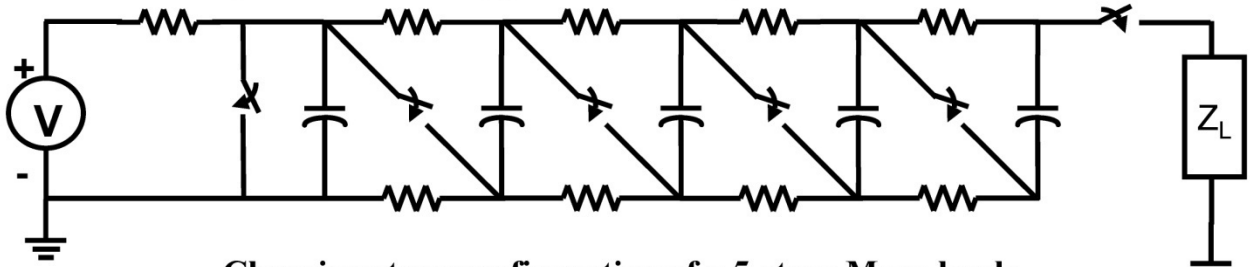
Basic Marx Generator

- Necessitates isolation elements between stages (R or L typically) that can hold off V
- Waveform subject to distortion
  - Reduced output voltage
  - Slow risetime
  - Impaired stage triggering

  Due to parasitic circuit elements
  - Capacitance
    - Stage-to-stage
    - Stage-to-ground
  - Inductance
    - Switch
    - Capacitor
    - Leads/layout

Marx Generators

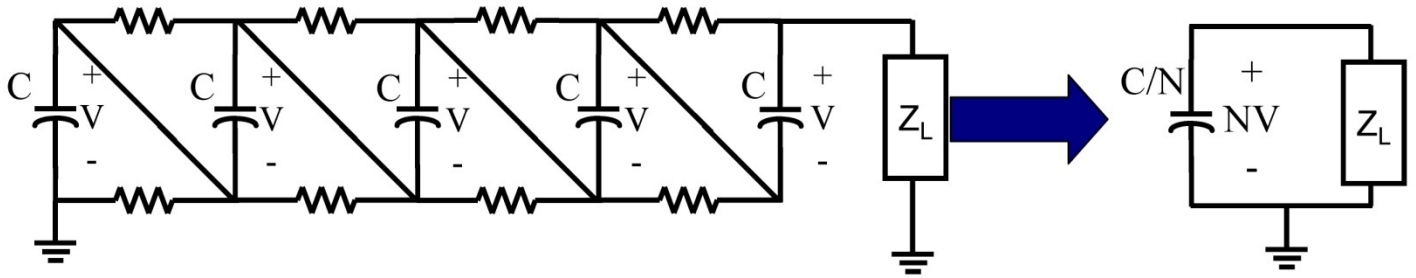
- Common voltage multiplier especially for high energy needs
- N=Number of stages
- V is the charging voltage
- Ideally, output voltage is NV
- Total energy $$W = \frac{1}{2} NCV^2 = \frac{1}{2} \frac{C}{N} (NV)^2$$
- Resistors serve two purposes
  - Determine the charging time of each stage
  - Decouple each stage when switches are closed
- Switches are closed sequentially
  - First stage or two are triggered externally



Charging stage configuration of a 5-stage Marx bank

Marx Generators

- Ideal case considering no parasitics
- Value of charging resistors must be less than the on-state resistance of the switches
- Output voltage is the response of a single capacitor, C/N, charged to NV switched into Z_L
  - For a purely resistive load, output voltage will have a $R_L(C/N)$ response



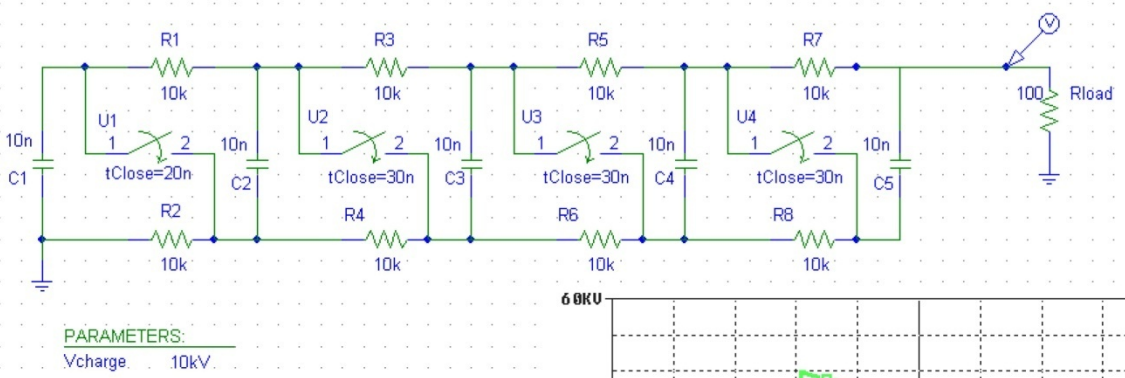
Erected stage configuration of a 5-stage Marx bank

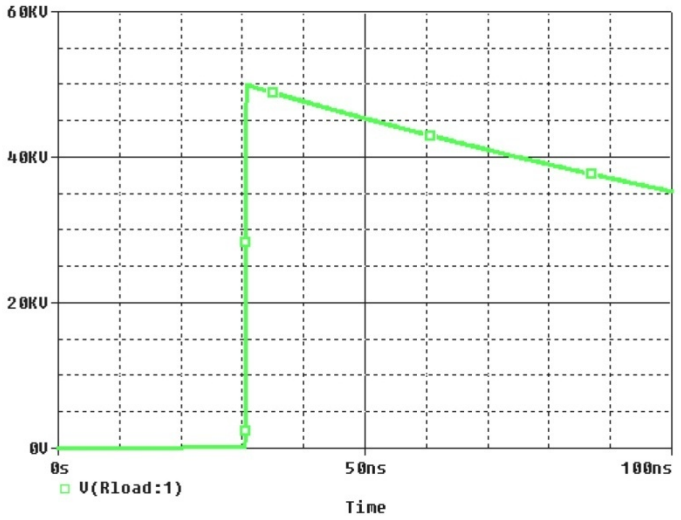
Equivalent Circuit

Impact of Parasitic Capacitance on Marx Voltage

Marx Generators

- Ideal case considering no parasitics

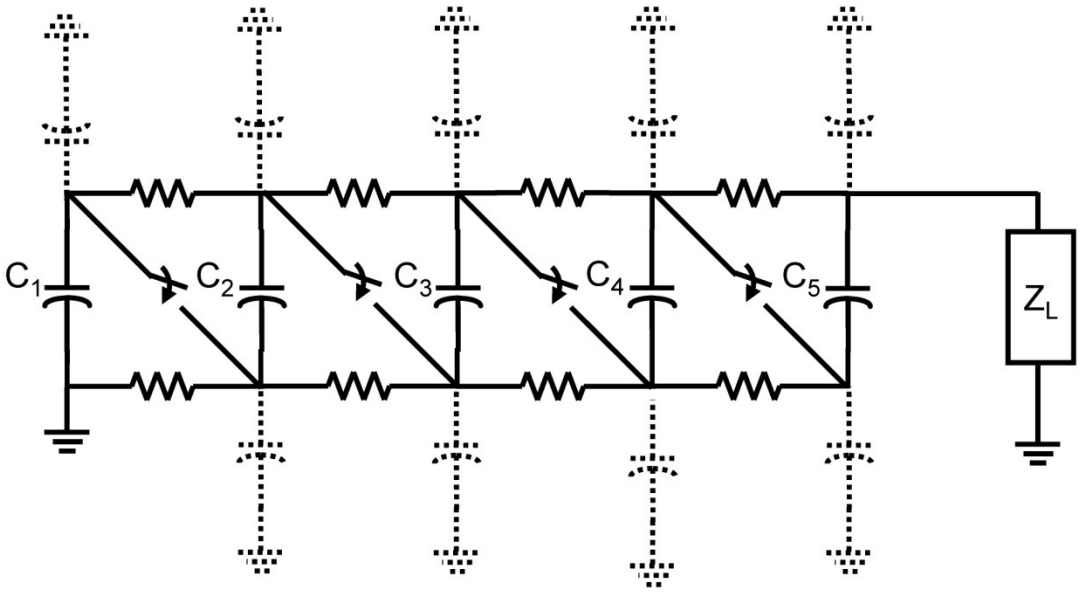




PSpice Simulation of an ideal 5-stage Marx generator

Impact of Parasitic Capacitance on Marx Voltage

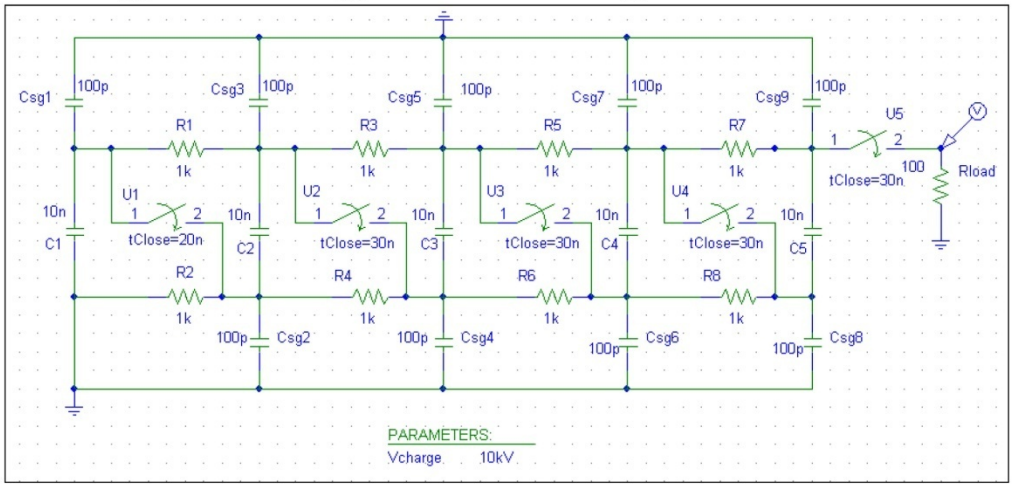
Stage to ground parasitics

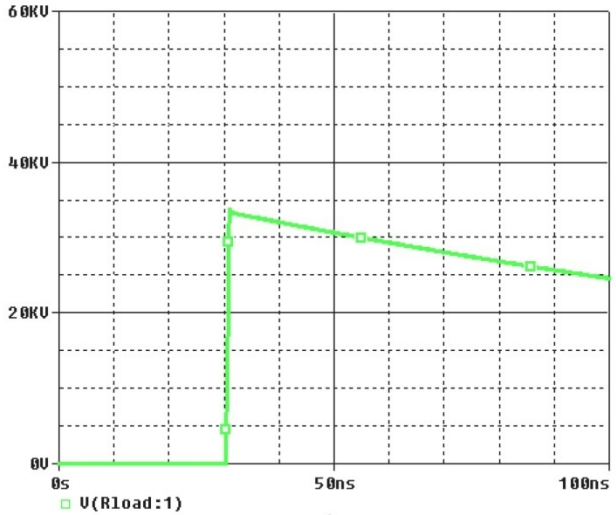


5-stage Marx Generator with stage to ground parasitics

Impact of Parasitic Capacitance on Marx Voltage

Stage to ground parasitics



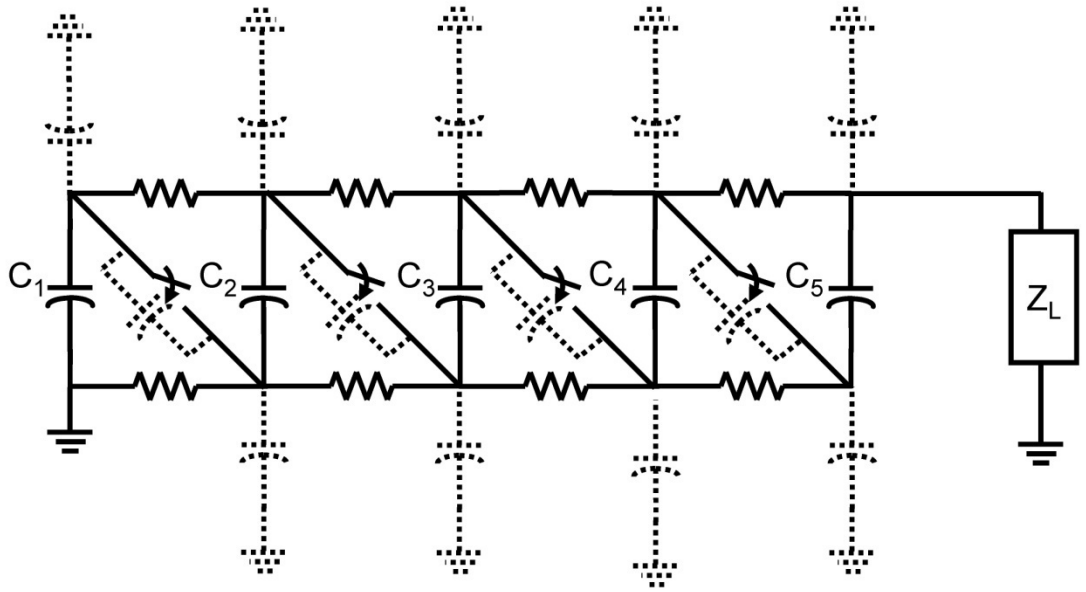


PSpice simulation of a 5-stage Marx Generator with stage to ground parasitics

2% parasitic capacitance reduces output voltage by 30%

Impact of Parasitic Capacitance on Marx Voltage

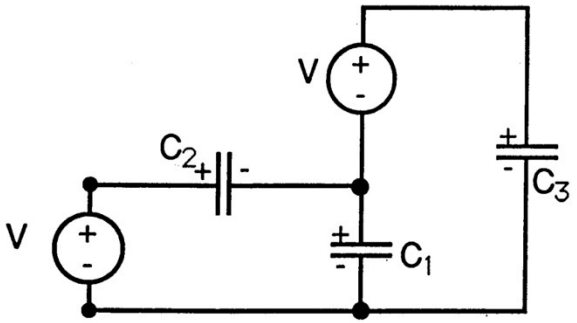
Stage to ground and gap parasitics



5-stage Marx Generator with stage to ground and gap parasitics

Impact of Parasitic Capacitance on Marx Voltage

Stage to ground and gap parasitics



C_1: stage to ground capacitance
C_2: gap capacitance
C_3: stage capacitance

$$V_{C_2} = \frac{C_1 + 2C_3}{C_1 + C_2 + C_3} V$$

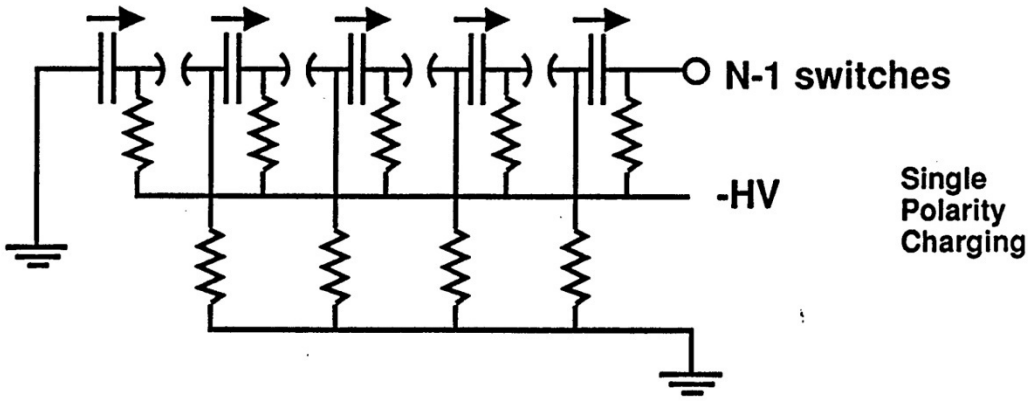
$$C_2 << C_1, C_3$$

$$V_{C_2} = \left(1 + \frac{C_3}{C_1 + C_3}\right) V < 2V$$

Switching behavior (i.e. voltage at spark gaps) depends on ratio of stray - C's!

Marx Charging Options

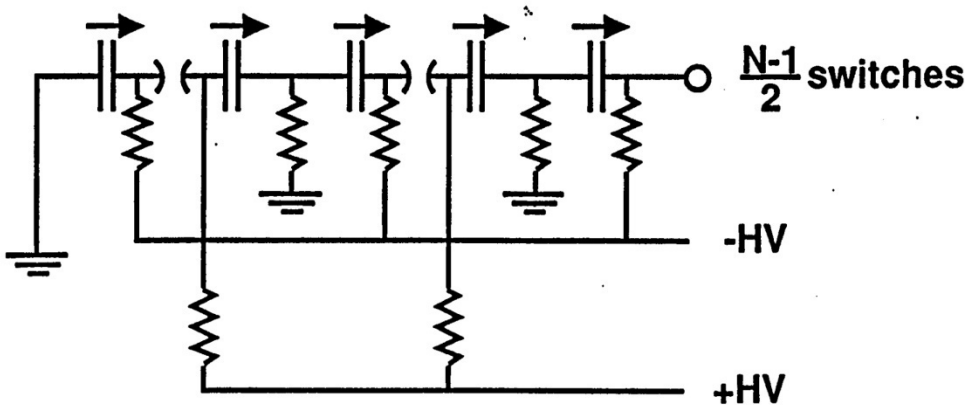
Single Polarity Charging Scheme



- Single polarity charging requires N-1 switches where N is the number of stages
- Above schematic employs negative charging
- 5-stage Marx requires 4 switches

Marx Charging Options (cont.)

Dual Polarity Charging Scheme

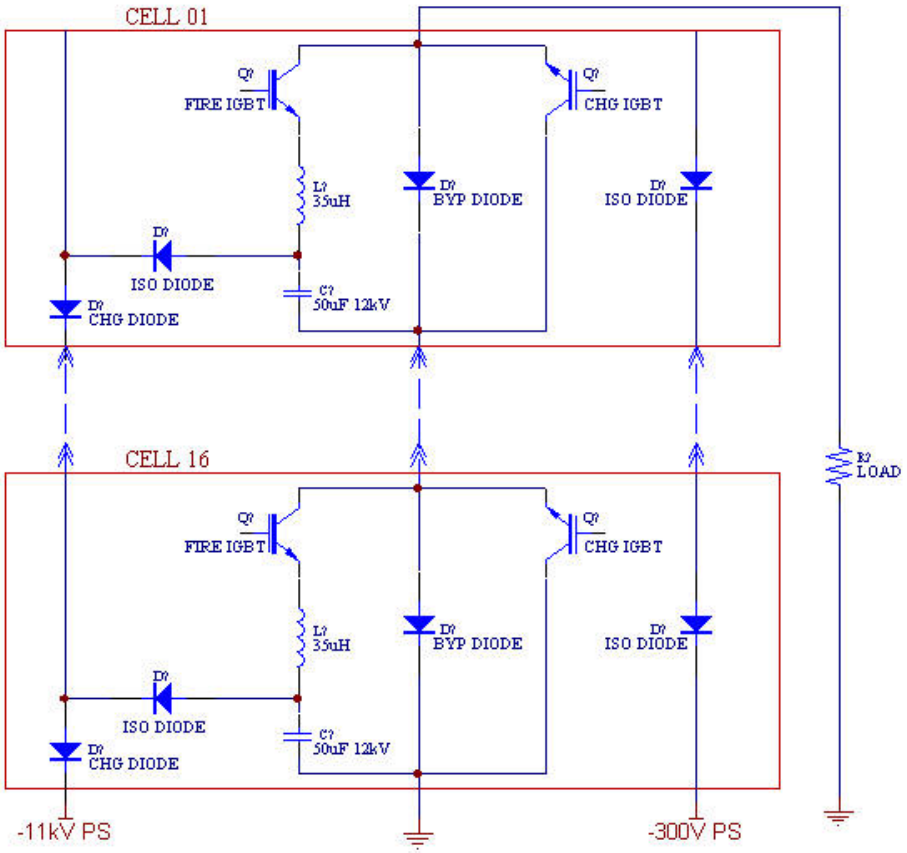


- Dual polarity charging requires (N-1)/2 switches where N is the number of stages
- 5 stage Marx above employs only 2 switches
- Switch reduction reduces jitter thereby improving performance

Solid State Marx

- Use as a voltage multiplier to array solid state switches to klystron voltage requirements
  - Output ~0.1 MV
  - Cells ~few kV
  - Square output waveform
    - Hard switch (close/open) topology
    - Controlled switching of each cell
  - High average power
  - High PRF (> Hz)
  - Long life
- Solid state charging/isolation elements
  - Low loss
  - Minimize recharge time

Simplified Schematic of ILC-Marx P1-Prototype



- Marx Topology: Charge Cells in Parallel, Discharge in Series
- 11kV per Cell
- 16 Cells
  - 11 prompt cells → 120 kV
  - 5 delay cells, compensates capacitor droop
- Cell High Voltage Switches
  - Array of 4.5kV, 60A IGBTs 3 parallel X 5 series
  - Fire switches erect Marx
  - Charge switches provide current return path for main charging supply (-11 kV) and auxiliary power (-300 V)
- Diode Strings Provide Isolation Between Cells When Marx Erects
  - 18 series 1200 V, 60A, Ultrafast Soft Recovery Type
  - Parallel Resistors and MOVs to balance & protect against over-voltage
- Inductors Limit Fault dI/dt

P1-Marx Cell Front & Rear Views

5 Charging SW Modules

5 Firing SW Modules

Charge Diode String

Bypass Diode String

Connector Group to Backplane

Cell Grounding Relay

Cap. Discharging Resistor

Equipotential Ring

Energy Storage Capacitors

Control Power Converters

11kV Isolated Power/Trigger Boards

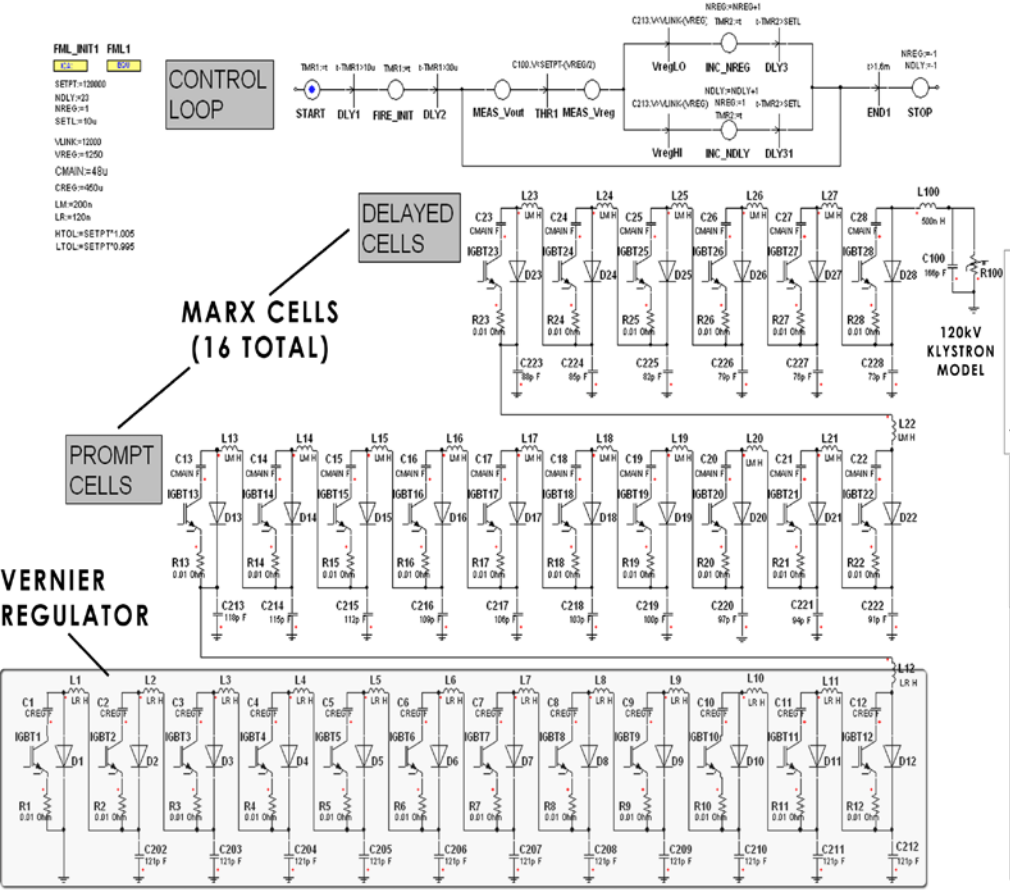
Cell Control Module

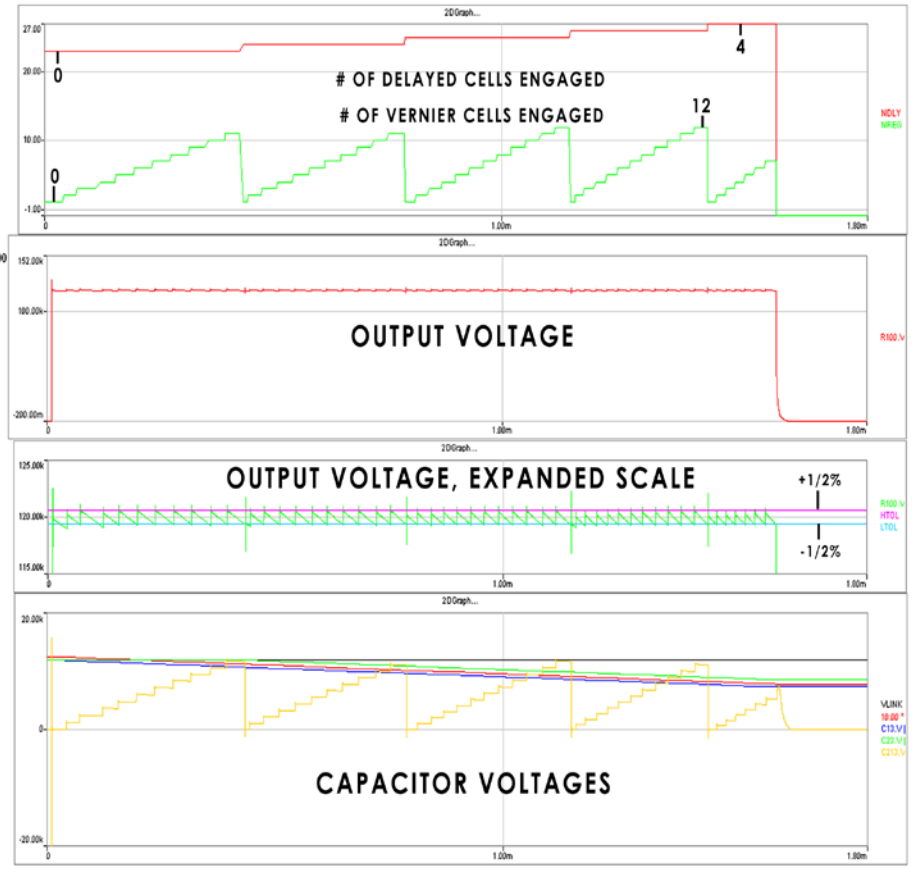
dI/dt Limiting Inductor

Charge Isolation Diode String

P1-Marx Installed in “Sealed” Enclosure

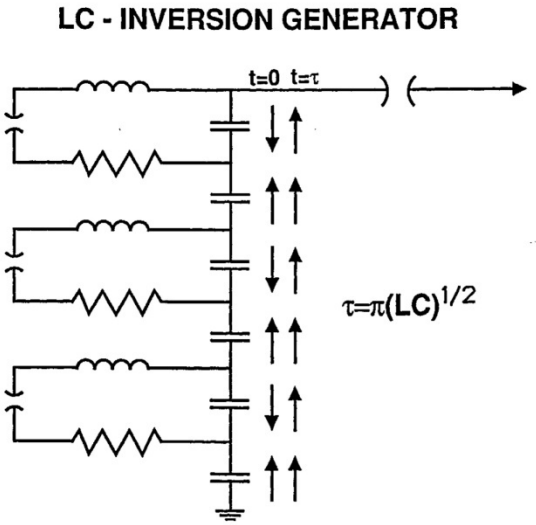
P1-Marx Voltage Regulation





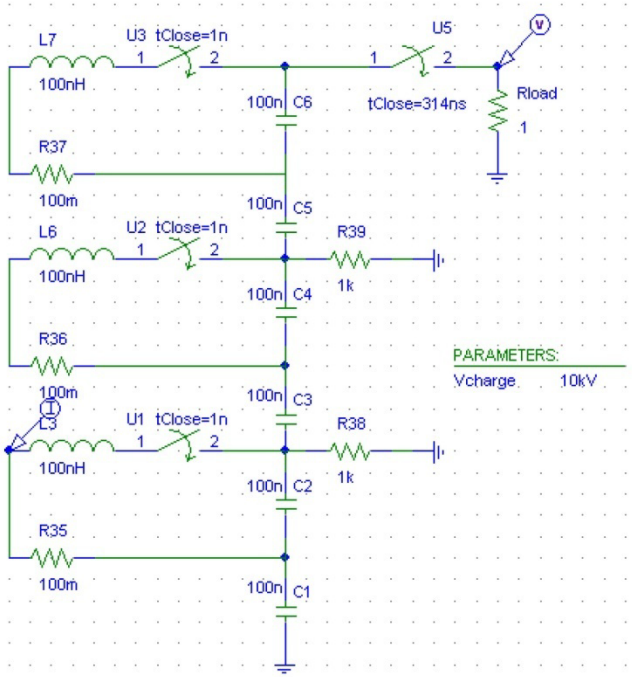
Inversion Generator

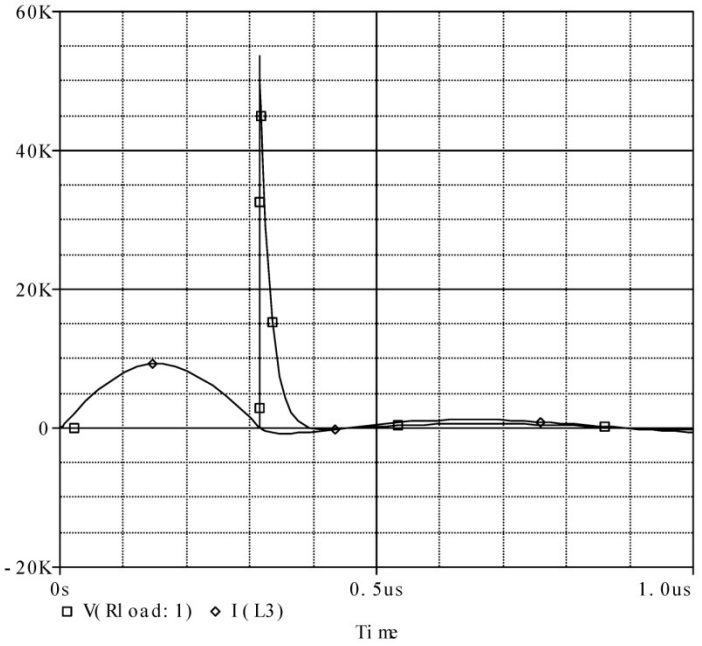
- Modified Marx Generator
- Primary Concept
  - A series arrangement of capacitors with alternating charge polarity of V volts are switched such that the polarity of every other capacitor is reversed resulting in NV output voltage
- Reduces number of switches by half
- Increases complexity by introducing timing issues



Marx Variant: Inversion Generator (cont.)

Inversion Generator



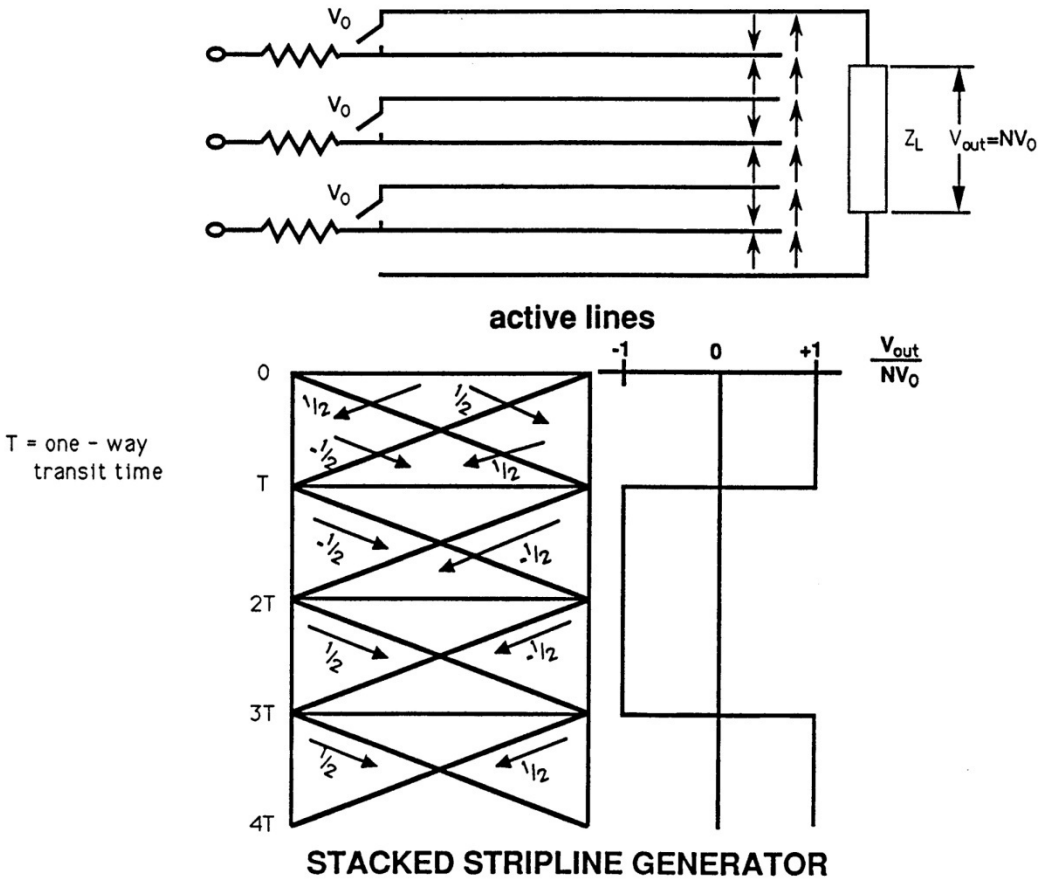


$$\tau = \pi(LC)^{1/2} = 314 \text{ nsec}$$

Pspice simulation of 6-stage LC Inversion Generator

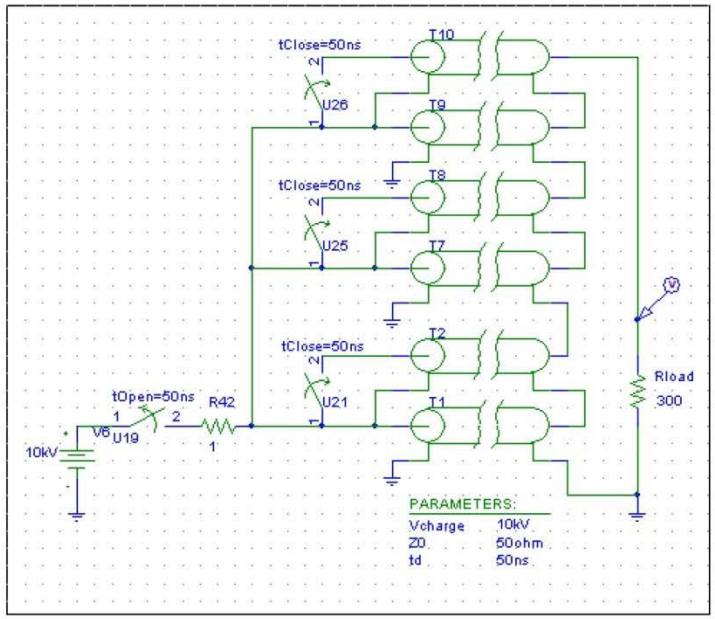
Marx-PFL Hybrid: Stacked Blumlein

Stacked Blumlein Generator

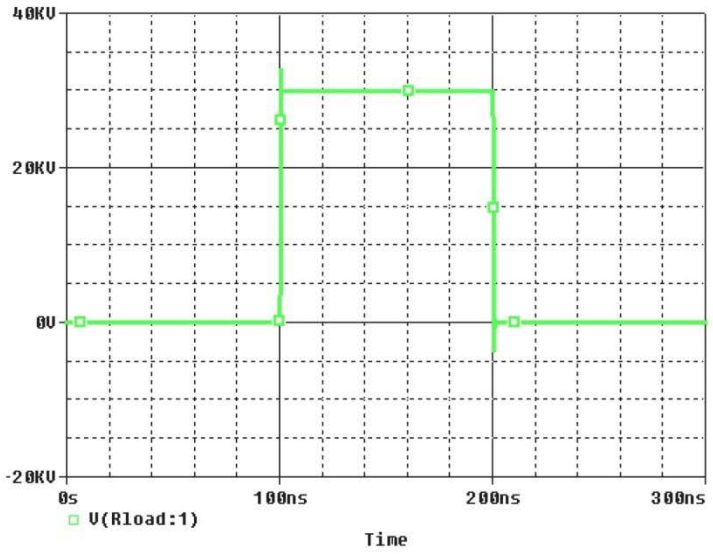


Marx-PFL Hybrid: Stacked Blumlein (cont.)

Stacked Blumlein Generator

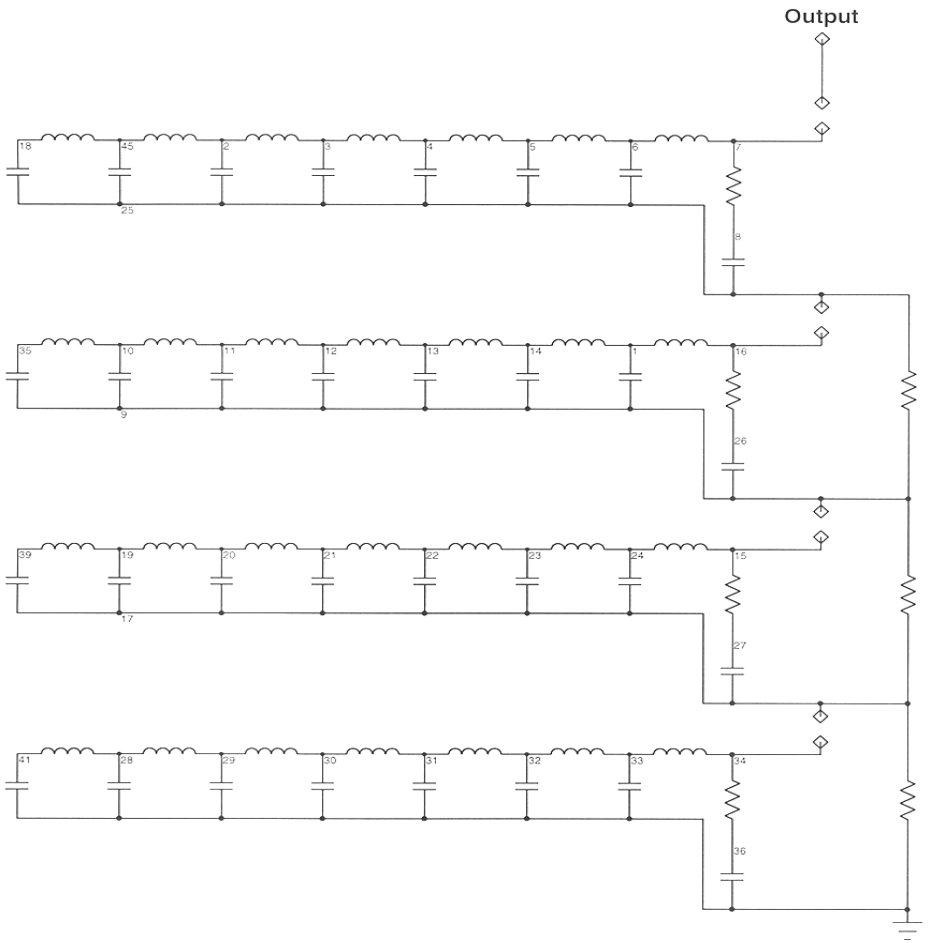


- 3 Stage Blumlein deliver 3X voltage multiplication
- Major drawback as number of stages increases so does the load impedance
- Matched conditions $R_{load} = 2NZ_0$ where N is the number of stages and Z_0 is the T-line impedance

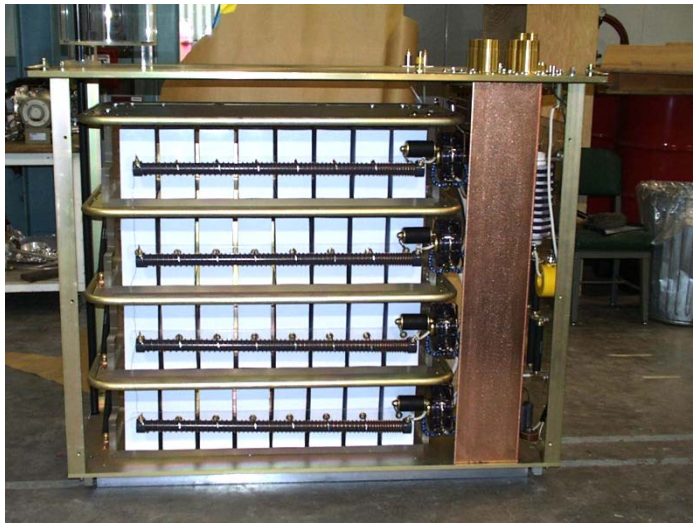


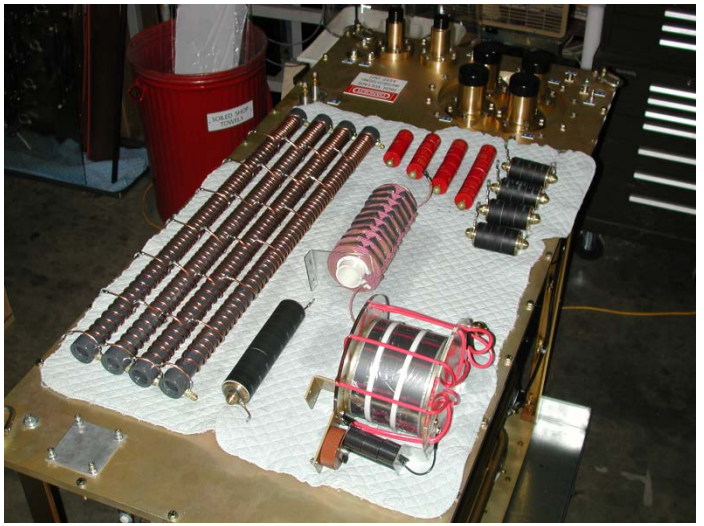
PFN Marx

- Matched condition: $Z_{load} = NZ_o$
- PFN waveform sensitive to parasitic capacitance and inductance
- It does work!
  - 4 stage
  - 7 section PFN
  - $Z_o = 5\ \Omega$



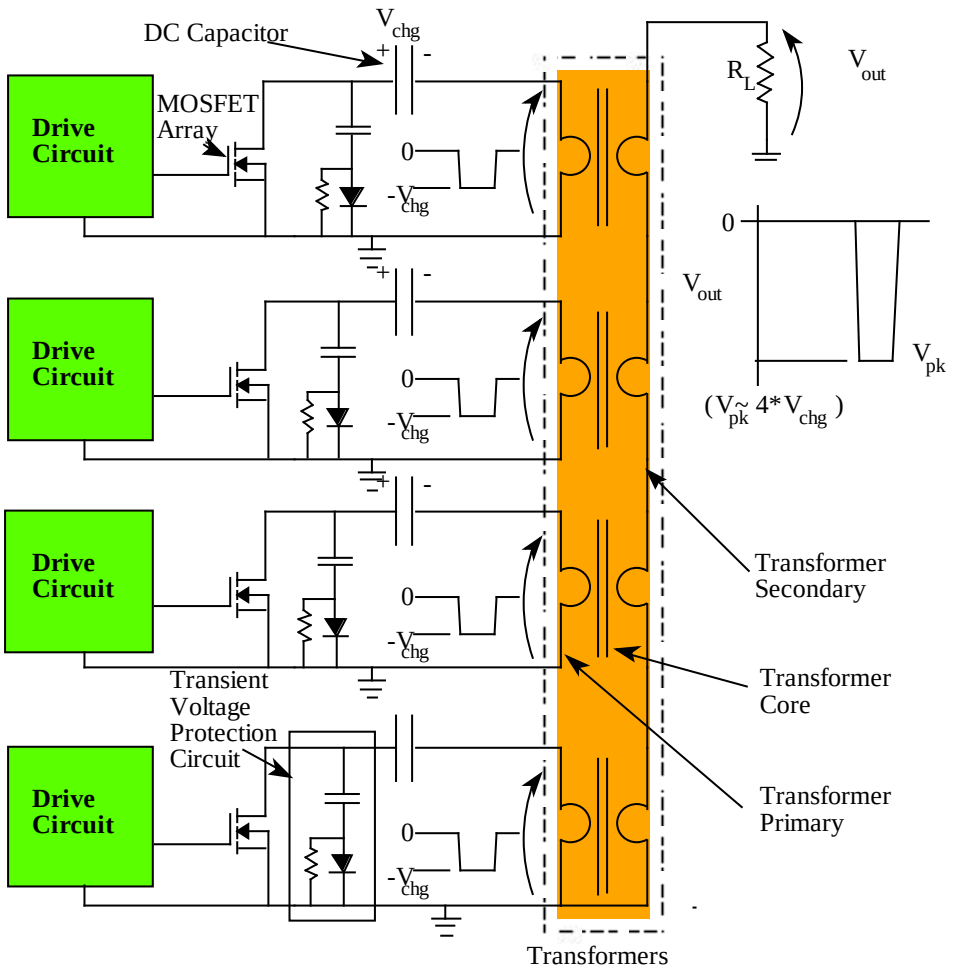
PFN Marx





Solid State Inductive Adder

- N identical low (limited by switch) voltage modules
  - Hard tube
    - MOSFET
    - IGBT
  - Linear amplifier
- Each module drives a single-turn high bandwidth output transformer
- The transformer secondaries are connected in series to inductively add the voltage of the individual modules
- Modules remain at ground potential throughout the pulse



Inductive adder concept - simplified schematic

Inductive Adder Topology - Advantages

- All drive components ground referenced
- No high voltage grading required (except transformer secondary)
- Pulse format defined by programmable pulse generator
  - Pulse width agility
  - Burst frequency agility
  - High burst frequency >1 MHz
- Modular - adder consists of stack of identical modules
  - All modules switch same voltage/current
  - All modules triggered simultaneously
  - Scaleable to higher voltages by adding modules
- Low source impedance
  - Can drive wide range of load impedance
  - Load voltage is essentially independent of load

Inductive Adder Topology - Issues

- Each module must switch full load current
  - May require many parallel components (switches, capacitors, etc.)
  - Parallel switching devices must have low jitter on both turn-on and turn-off
- Requires very low inductance in primary circuit
- Requires very fast opening switch that can interrupt full load current and survive fault currents
- Fault currents can be very large
- Cost
- Complexity

Inductive Adder Design Considerations

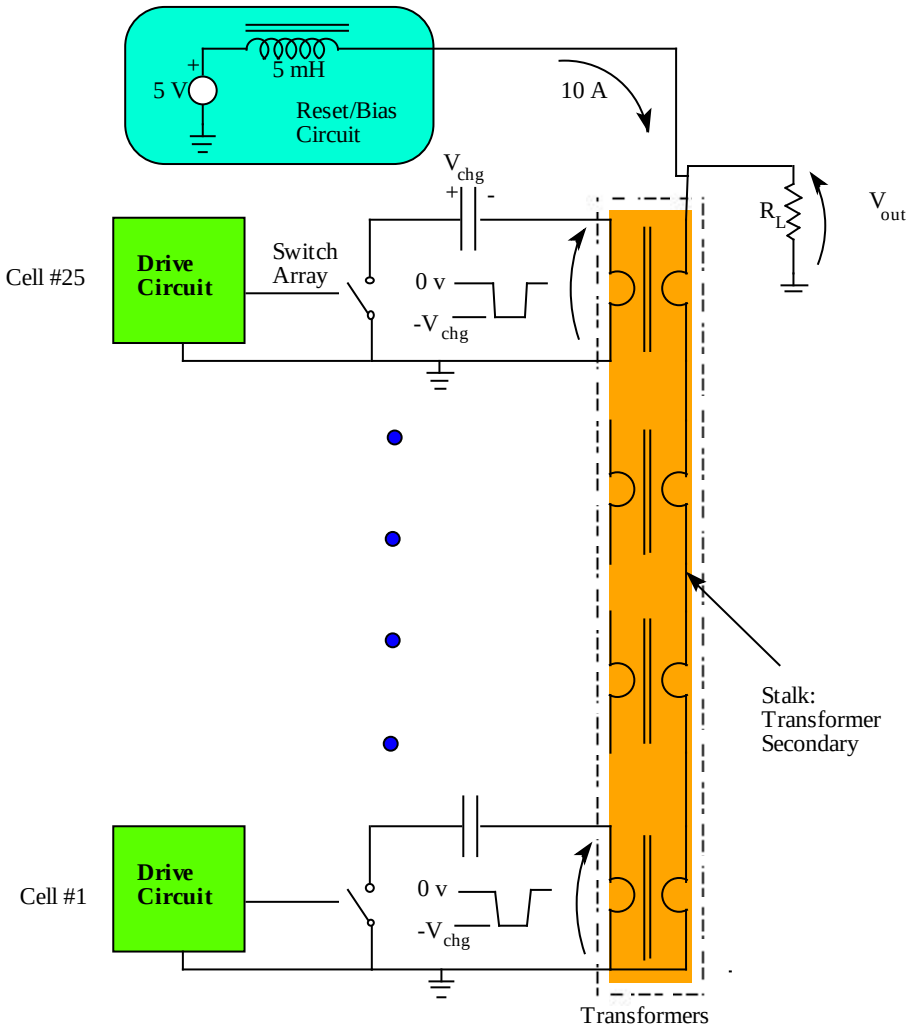
- Select Switch and switch drive circuit
  - Switching speed for both turn-on and turn-off
  - Maximum operating voltage (determines number of modules)
  - Current Rating (determines number of parallel devices)
- Size the capacitor (bank)
  - Must be large enough to meet droop requirements
  - Inductance must be low
  - Low ESR (equivalent series resistance)
- Design the pulse transformer
  - Core area must be sufficient for application
    - Total volt-seconds for single pulse if reset between pulses
    - Total volt-seconds for all pulses in burst if reset between bursts

Inductive Adder Design Considerations

- Make sure that primary circuit inductance is minimized
  - Voltage drop across loop inductance during high di/dt affects load voltage
  - Energy stored in loop inductance can appear as voltage across switch
  - Include component inductance, transformer leakage inductance, and inductance of circuit board traces
- Protection circuits for switches
  - Overvoltage from $(L\ dI/dt)_{primary}$ on turn off
  - Overcurrent; load faults, transformer saturation
- Reset of adder magnetic core
  - Duty cycle sets minimum ratio for V_{reset}/V_{output} (total $V\tau = 0$)
- Recharge of capacitor between pulses/bursts
  - Interpulse recharge can reset core if voltage and current high enough

Inductive Adder Core Reset/Bias Circuit

- Voltage induced into the primary resets the magnetic core material between bursts
- H-field created by the DC current biases the magnetic cores to a single point on the BH curve.
- Reset through the secondary winding resets all the cores
- The series inductor protects and isolates the power supply from the high voltage output pulse
- Other reset circuits can be used: DC reset through the primary, pulsed current into either the primary or secondary



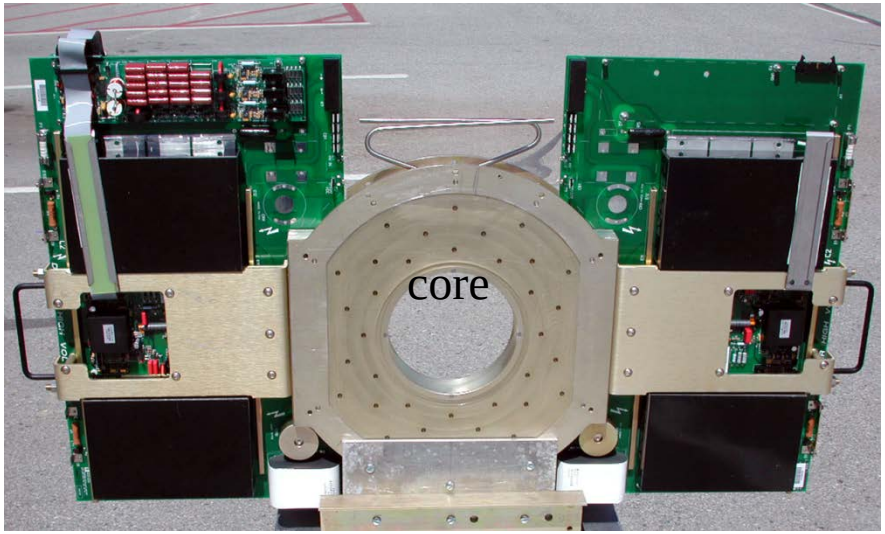
NLC Solid-State Inductive Adder Modulator

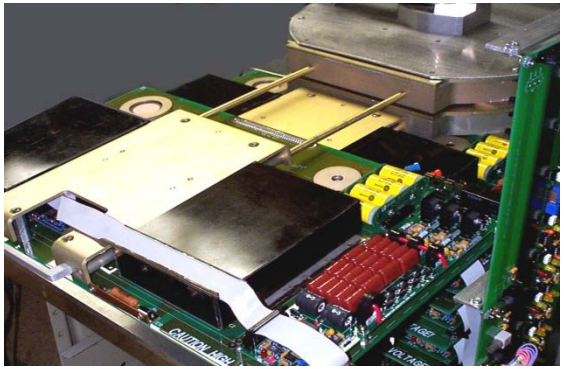
- Modulator Requirements:
  - Output Voltage 500kV @ 2kA
  - Pulse-width - 3μs
  - Klystron Efficiency > 80% (rise & fall times less than 400 ns)
  - Repetition Rate - 120 Hz (500kW Average)
  - Lifetime - 30 years
  - Cost < 200k$/ Modulator
  - Each modulator drives 8 klystrons

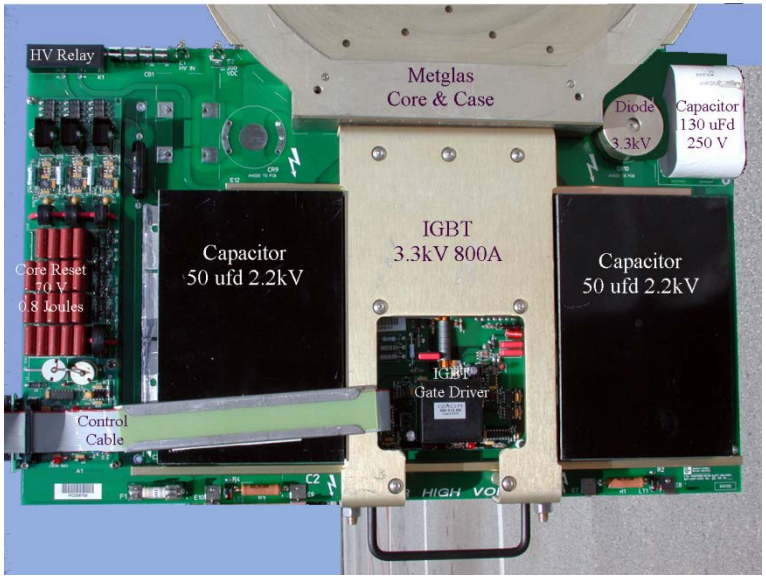
NLC Solid-State Inductive Adder Modulator

- Fractional turn pulse transformer multiple parallel primaries, each ground referenced
  - 500 kV, 2080 A, 1040 MW, 3.2μs, 500 kW average
  - 76 single turn primaries
  - Low loss Metglas cores
  - 3 turn secondary connects all cores in series
  - 152 IGBT switches (two per primary)
    - Rating: 3.3 kV, 800 A rms
    - Operating point: 2.2 kV, 3.2 kA
- Major concerns
  - Klystron protection when there are internal faults
  - IGBT protection when load faults (requires active sense and control circuitry)

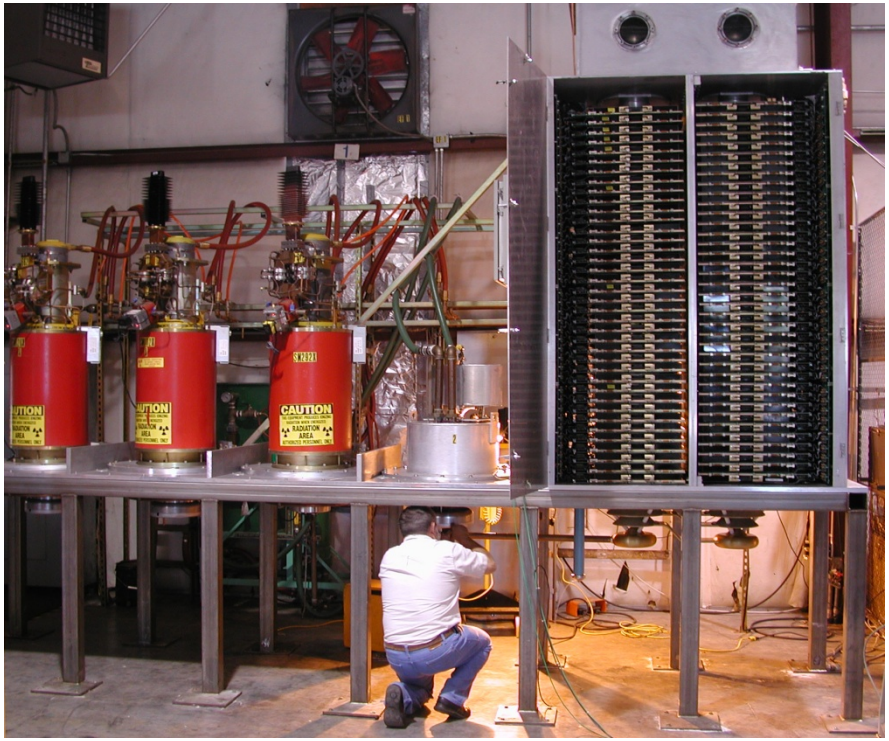
IGBT Drivers and Core



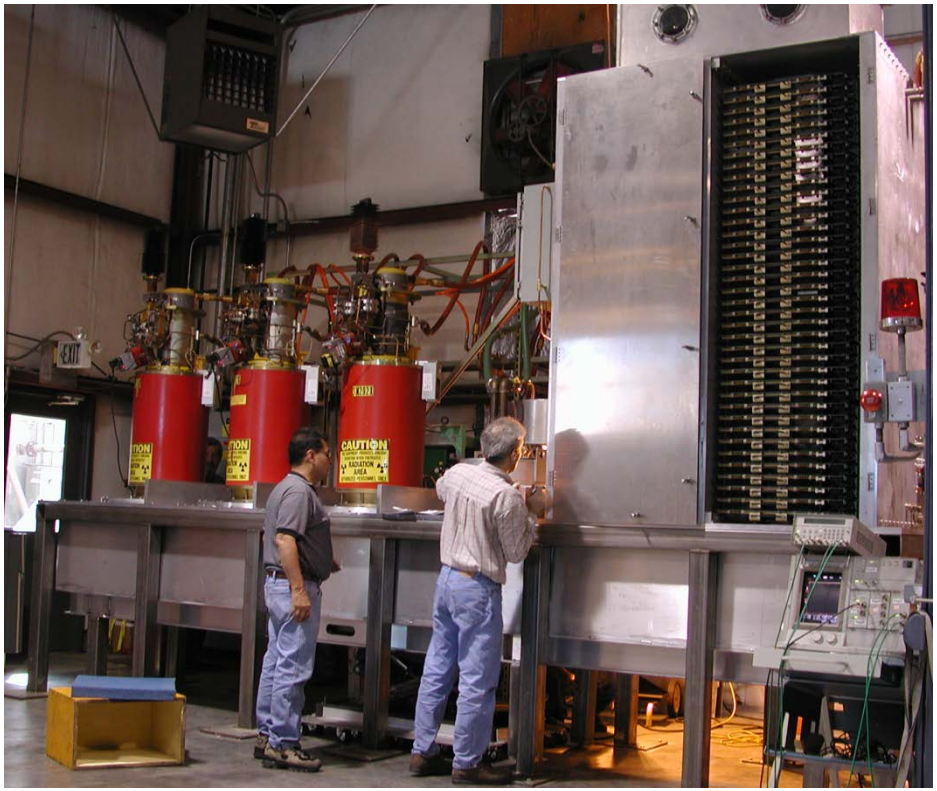




Prototype NLC Solid State Induction Modulator

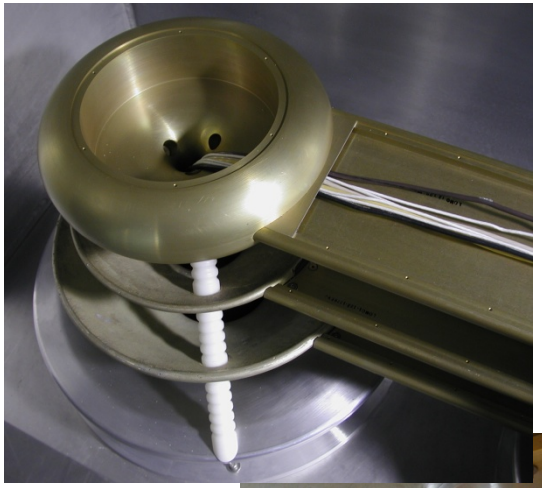


3 turn Secondary with water load

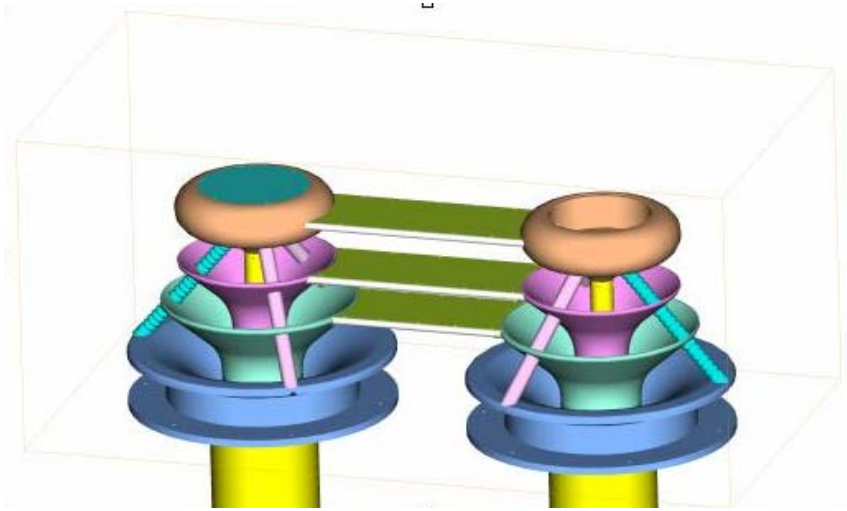


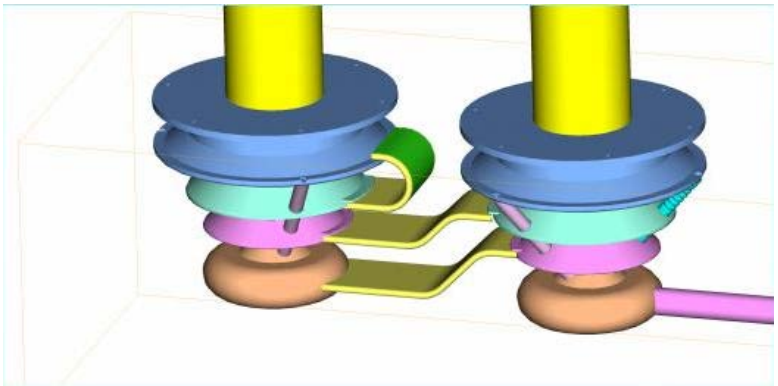
With oil tank installed

Prototype NLC Solid State Induction Modulator



- Coaxial Three Turn Secondary End Connection



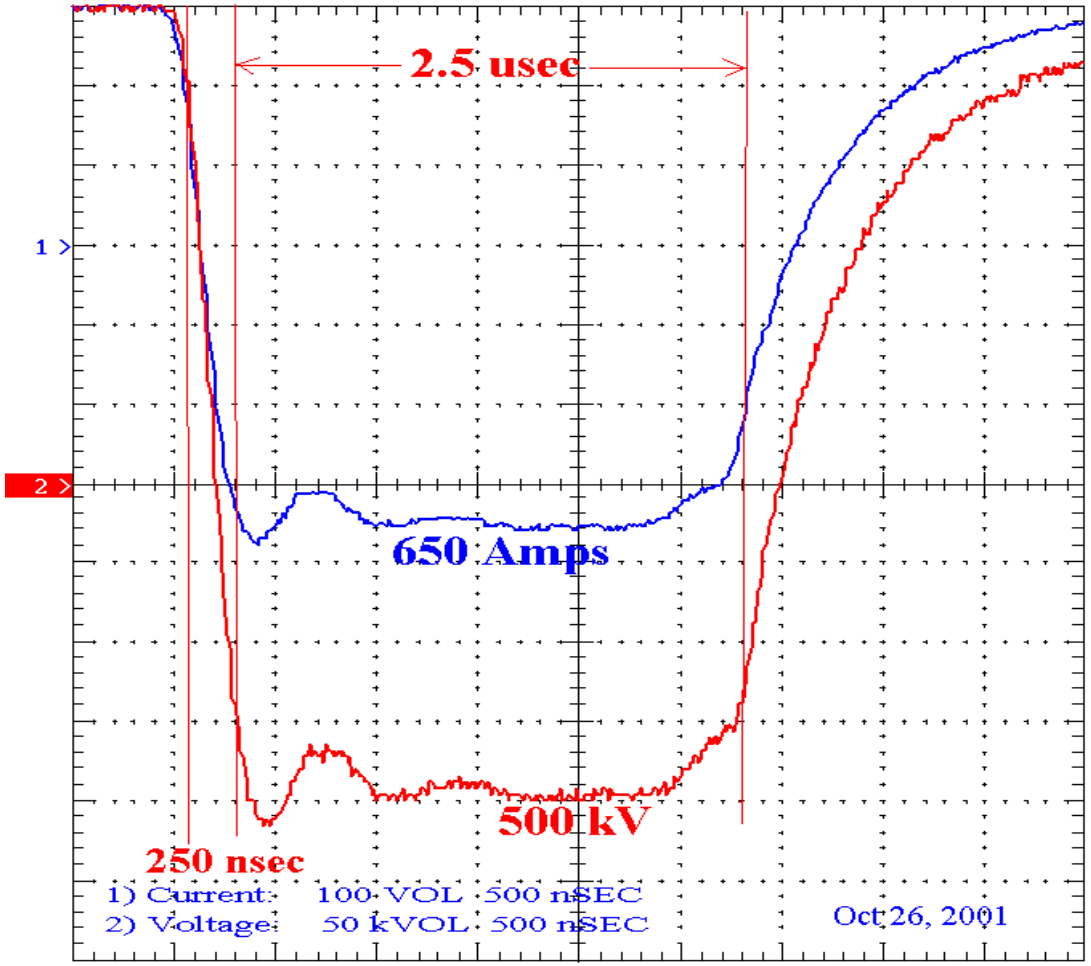


Prototype NLC Induction Modulator Pulse (Water Load)

Three Turn Secondary

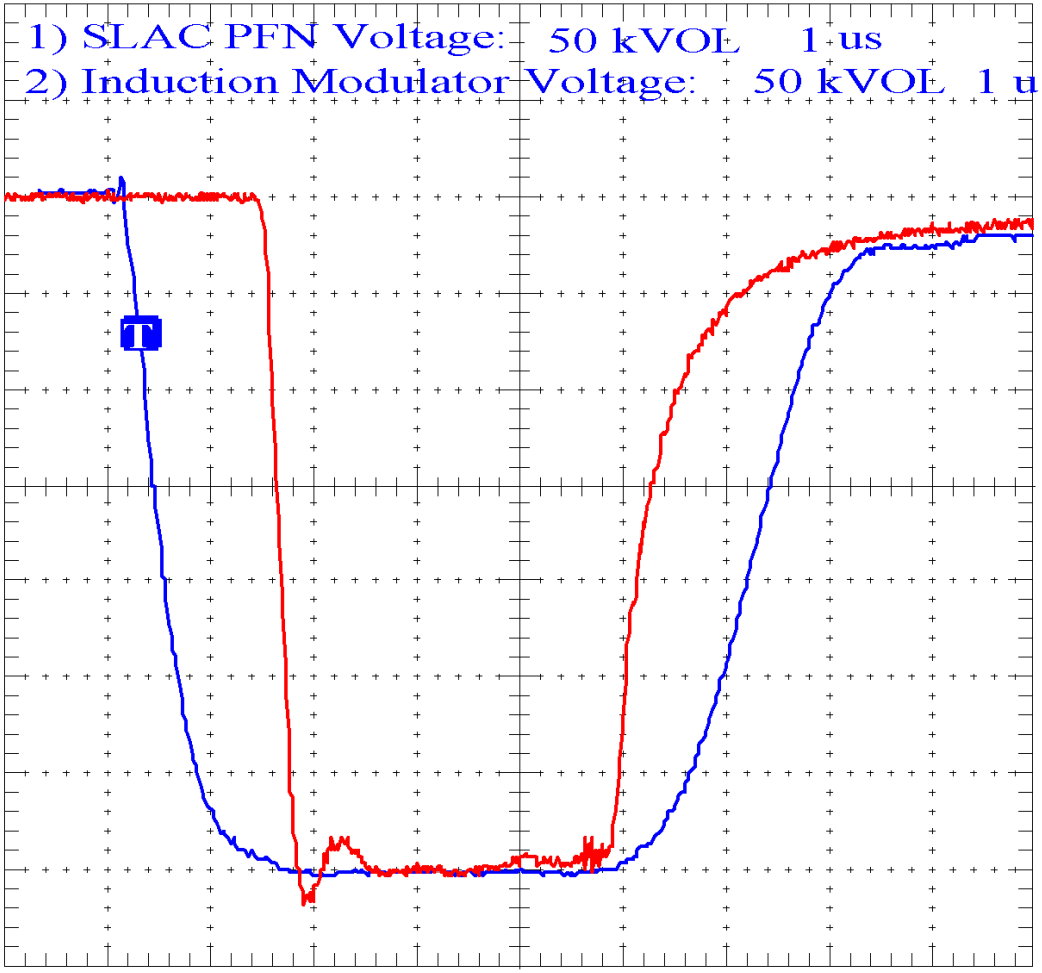
76 Metglas cores

152 IGBT Drivers

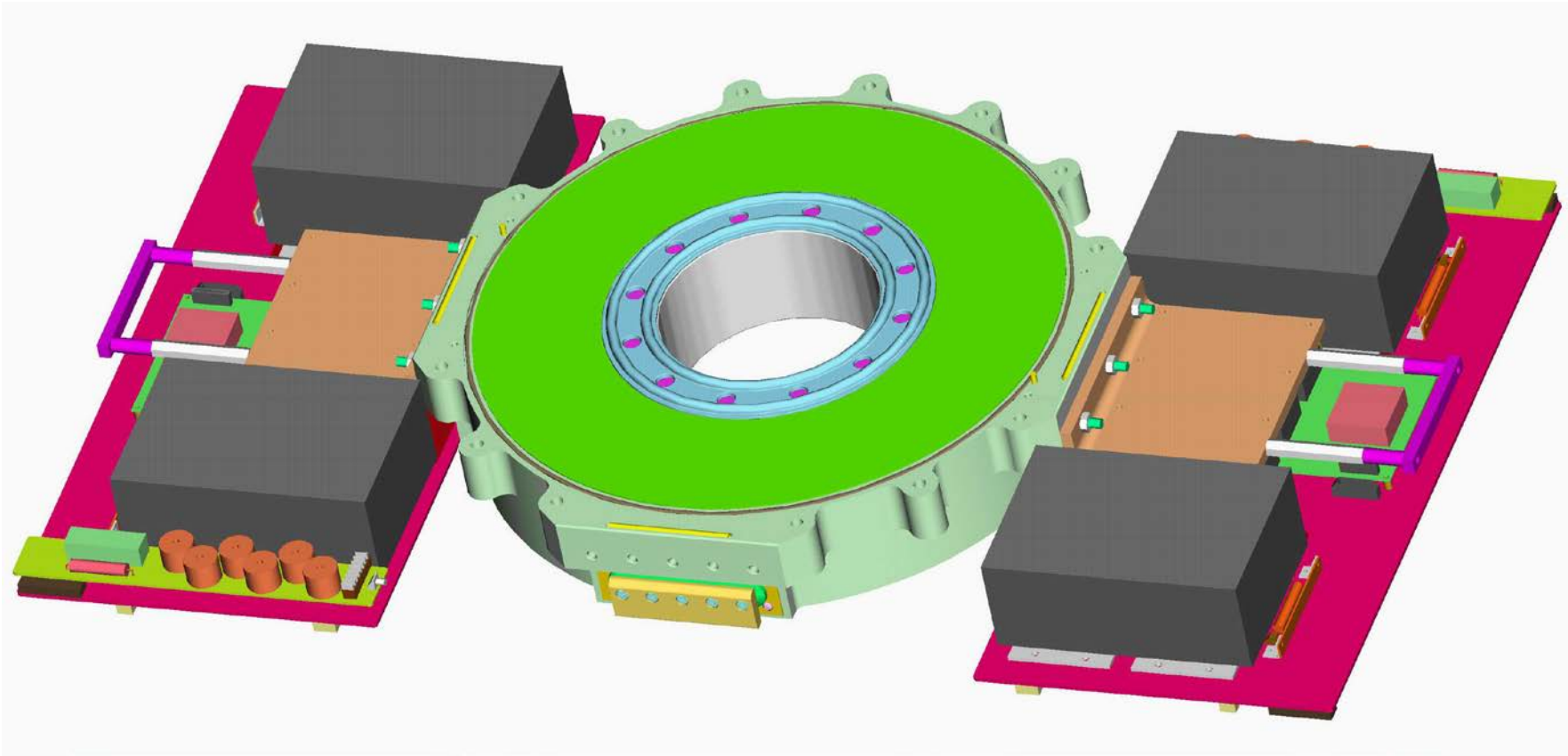


Comparison: Voltage Pulse of Induction Modulator vs. PFN

Nominal voltage: 350 kV
PFN: 375 A
Adder: 750 A
Overall adder efficiency >80%

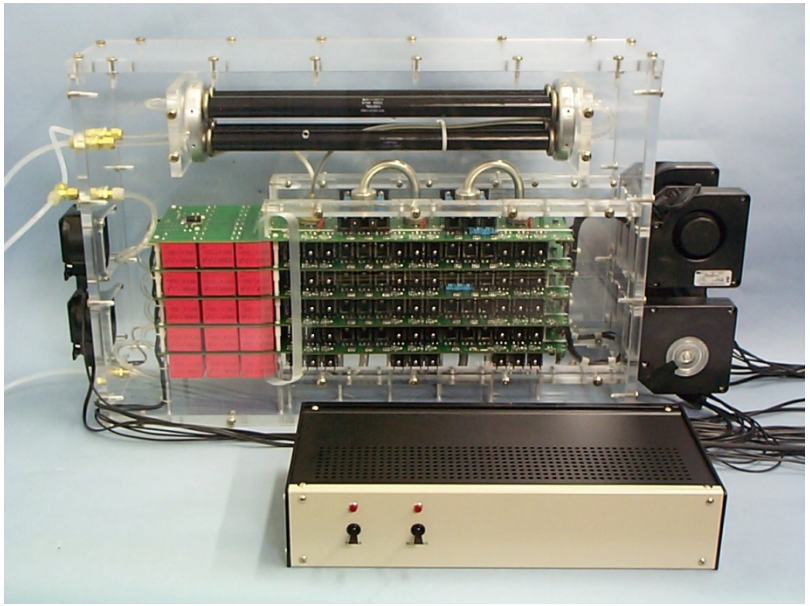


2-Pack Adder Cell w/Drive Boards (with 6.5kV IGBTs)

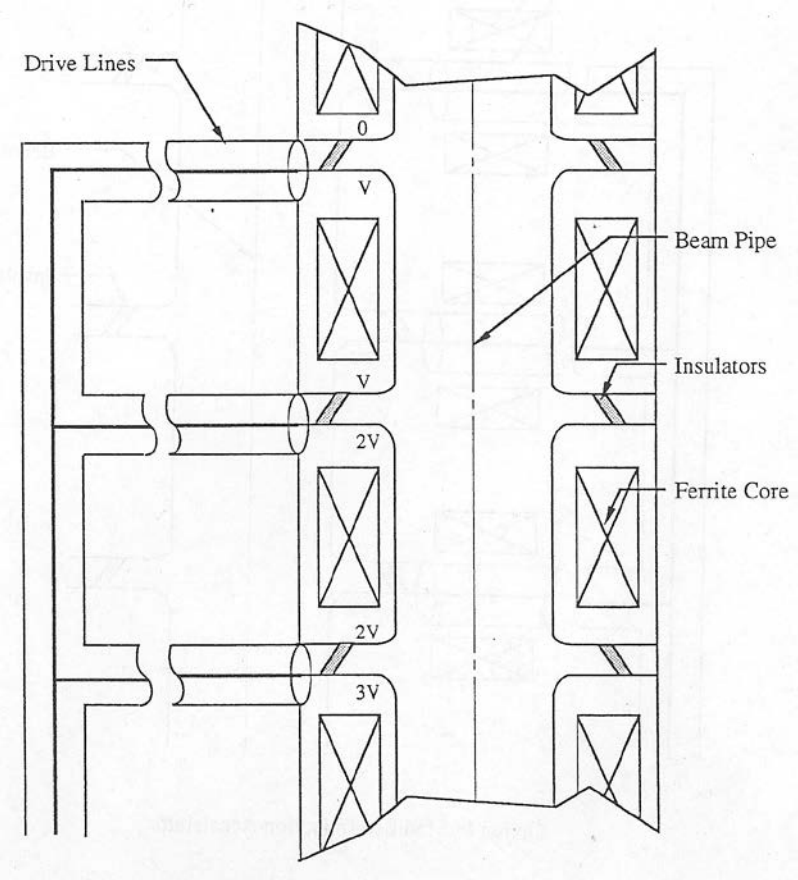


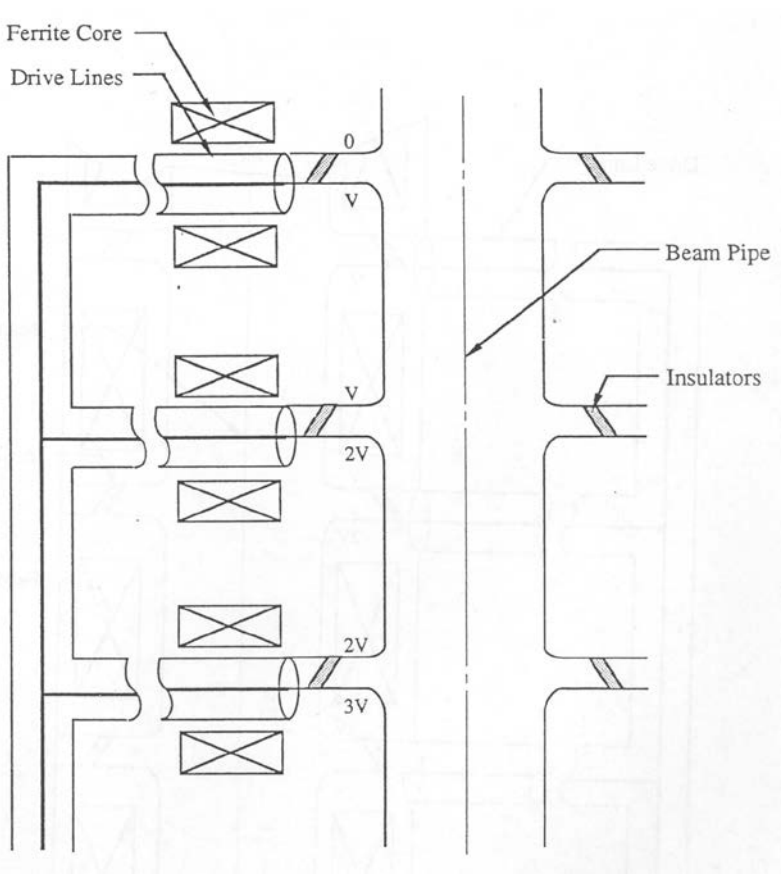
Commercial Inductive Adder Modulator

- 20 kV
- 100A
- 100 ns pulse, ~15 ns rise/fall
- To 25 kHz
- To 3 kW

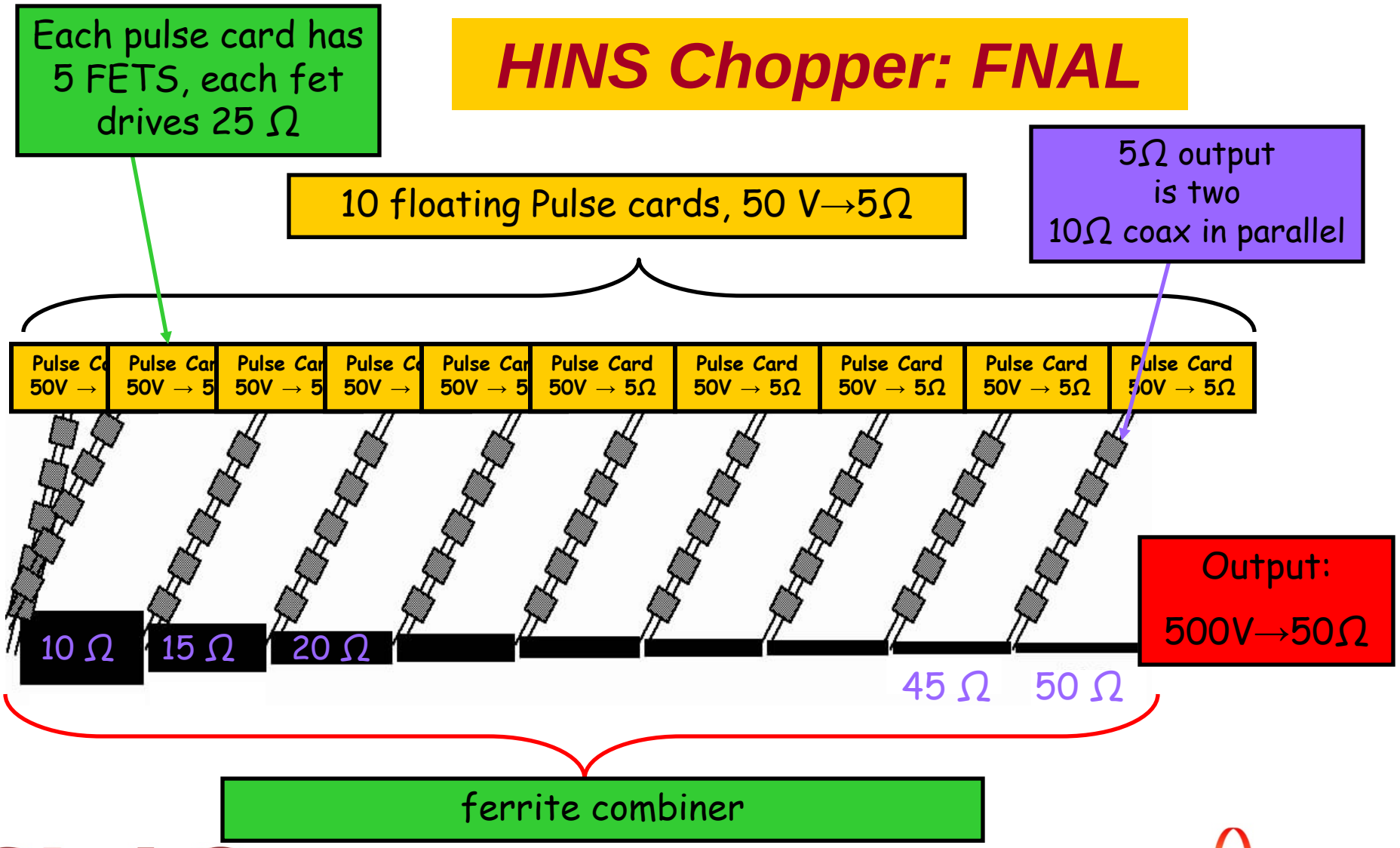


Transformation: Inductive to Transmission Line Adder (D Birx)

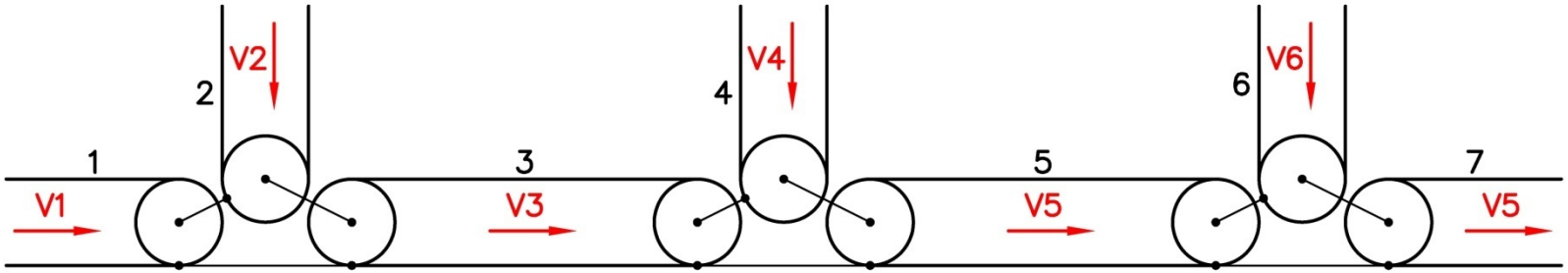


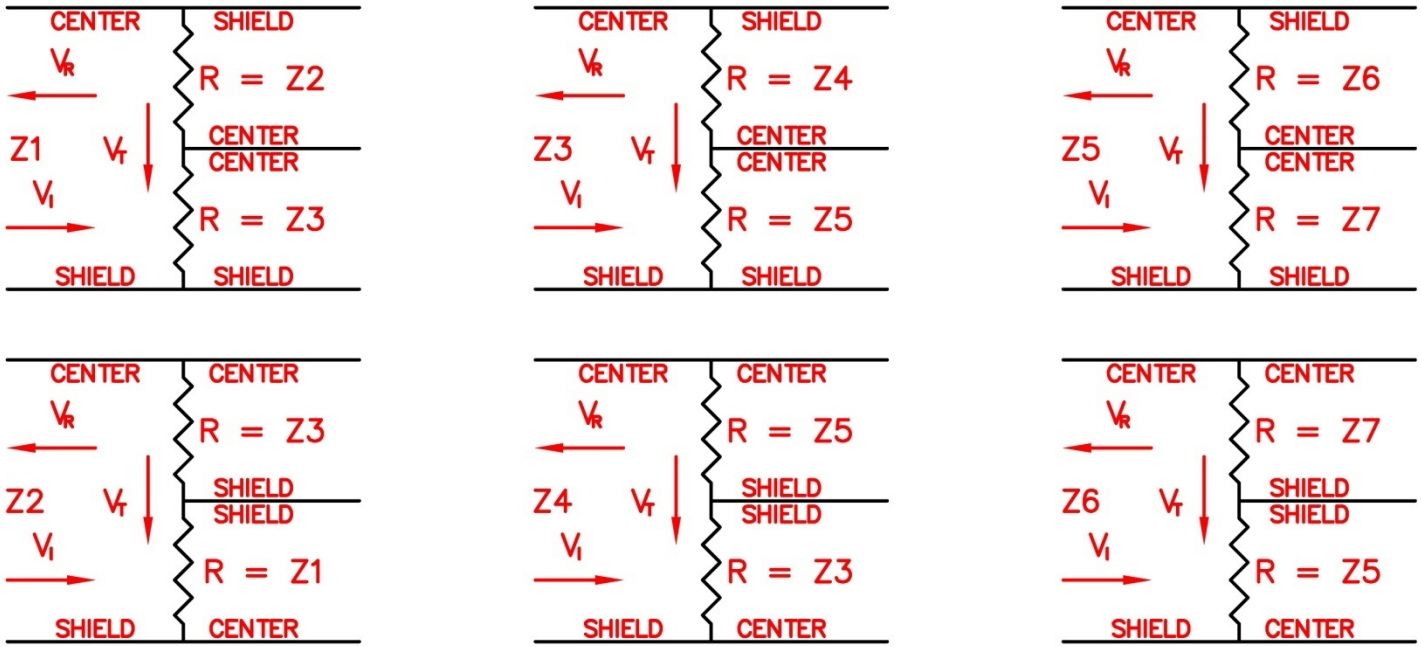


Transmission Line Adder Scheme: Cartoon



Transmission Line Adder Analysis





Transmission Line Adder Analysis (cont.)

- Transmitted wave: $V_T/V_I = (2\ R) / (R + Z_O)$
- Reflected wave: $V_R/V_I = [(R - Z_O) / (R + Z_O)]$
- Junction of lines 1, 2, & 3
  - $(V_T/V_I)_1 = (V_T/V_I)_2 = (2)(15)/(15 + 5) = 3/2$
    - Of the wave transmitted from 1: 1/3 → 2 and 2/3 → 3 by resistive division
    - Of the wave transmitted from 2: 1/3 → 1 and 2/3 → 3 by resistive division
  - $(V_R/V_I)_1 = (V_R/V_I)_2 = (15 - 5)/(15 + 5) = 1/2$
  - Line 1: $V_R = V_{R1} - (1/3)V_{T2}$ (center to shield) $= V_{I1}/2 - (1/3)(3V_{I2}/2) = 0$ if lines 1 and 2 carry the same waveform
  - Line 2: $V_R = V_{R2} - (1/3)V_{T1}$ (shield to center) $= V_{I2}/2 - (1/3)(3V_{I1}/2) = 0$
  - Line 3: $V_I = (2/3)V_{T1} + (2/3)V_{T2} = (1/3)(3V_{I1}/2) + (1/3)(3V_{I2}/2) = V_{I1} + V_{I2}$

Transmission Line Adder Analysis (cont.)

- Junction of lines 3, 4, & 5
  - $(V_T/V_I)_3 = (2)(5 + 15)/(5 + 15 + 10) = 4/3$
    - Of the wave transmitted from 3: 1/4 → 4 and 3/4 → 5 by resistive division
  - $(V_T/V_I)_4 = (2)(15 + 10)/(15 + 10 + 5) = 5/3$
    - Of the wave transmitted from 4: 2/5 → 3 and 3/5 → 5 by resistive division
  - $(V_R/V_I)_3 = (20 - 10)/(20 + 10) = 1/3$
  - $(V_R/V_I)_4 = (25 - 5)/(25 + 5) = 2/3$
  - Line 3: $V_R = V_{R3} - (2/5)V_{T4}$ (center to shield) $= V_{I1}/3 - (2/5)(5V_{I4}/3) = 0$ if line 3 carries a waveform that is 2X of line 4
  - Line 4: $V_R = V_{R4} - (1/4)V_{T3}$ (shield to center) $= 2V_{I4}/3 - (1/4)(4V_{I3}/3) = 0$
  - Line 5: $V_I = (3/4)V_{T3} + (3/5)V_{T4} = (3/4)(4V_{I3}/3) + (3/5)(5V_{I5}/3) = V_{I3} + V_{I4}$

Transmission Line Adder Analysis (cont.)

- Junction of lines 5, 6, & 7
  - $(V_T/V_I)_5 = (2)(25)/(25 + 15) = 5/4$
    - Of the wave transmitted from 5: 1/5 → 6 and 4/5 → 7 by resistive division
  - $(V_T/V_I)_6 = (2)(35)/(35 + 5) = 7/4$
    - Of the wave transmitted from 6: 3/7 → 5 and 4/7 → 7 by resistive division
  - $(V_R/V_I)_5 = (25 - 15)/(25 + 15) = 1/4$
  - $(V_R/V_I)_6 = (35 - 5)/(35 + 5) = 3/4$
  - Line 5: $V_R = V_{R5} - (3/7)V_{T6}$ (center to shield) $= V_{I5}/4 - (3/7)(7V_{I6}/4) = 0$ if line 5 carries a waveform that is 3X of line 6
  - Line 6: $V_R = V_{R6} - (1/5)V_{T5}$ (shield to center) $= 3V_{I6}/4 - (1/5)(5V_{I5}/4) = 0$
  - Line 7: $V_I = (4/5)V_{T3} + (4/7)V_{T4} = (4/5)(5V_{I5}/4) + (4/7)(7V_{I6}/4) = V_{I5} + V_{I6}$
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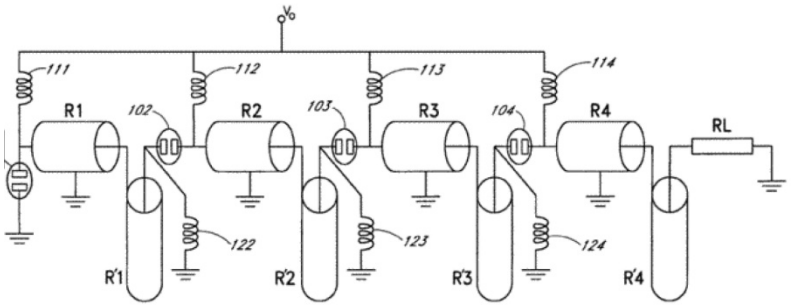
-
-

Where TL Adder & Blumlein Collide: Sparktronics Multi-stage Blumlein



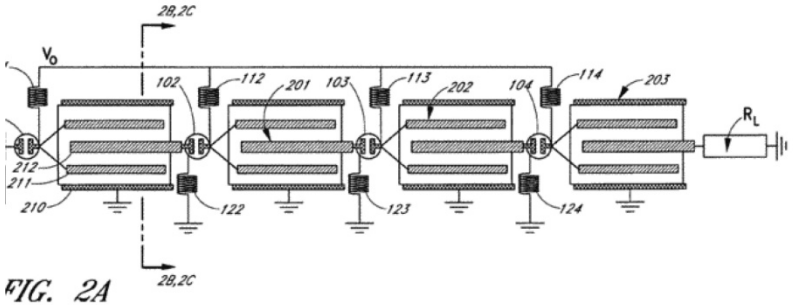


FIG. 2A

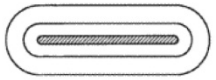


FIG. 2B

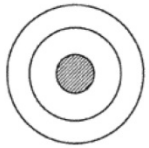
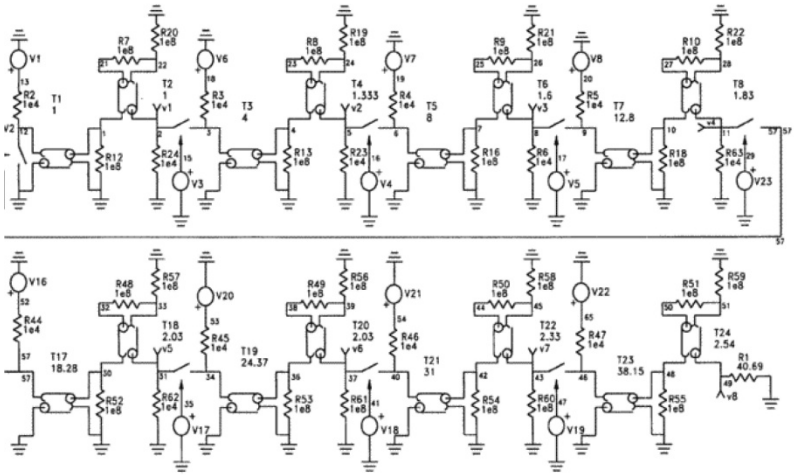
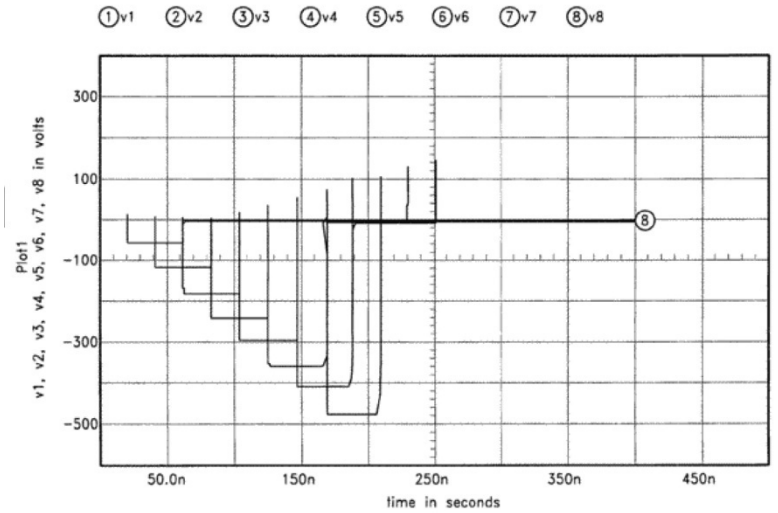


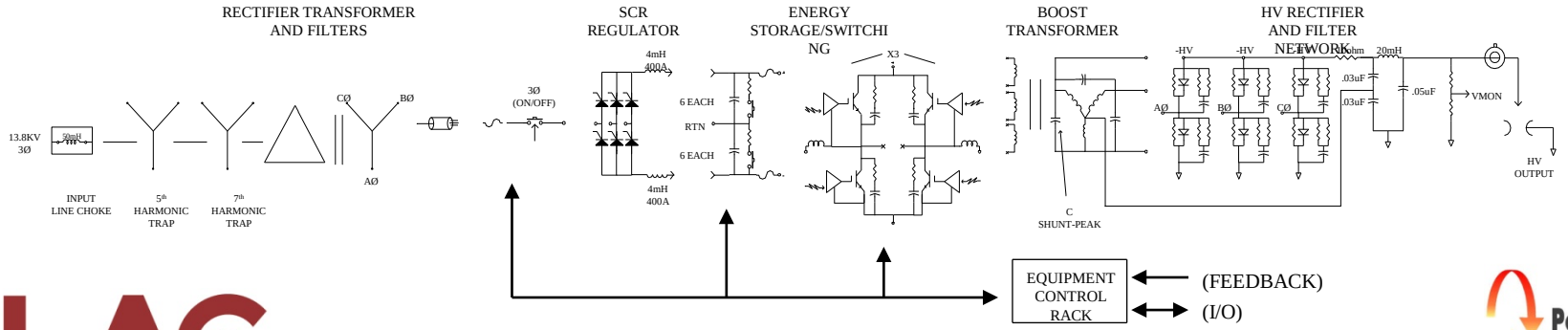
FIG. 2C





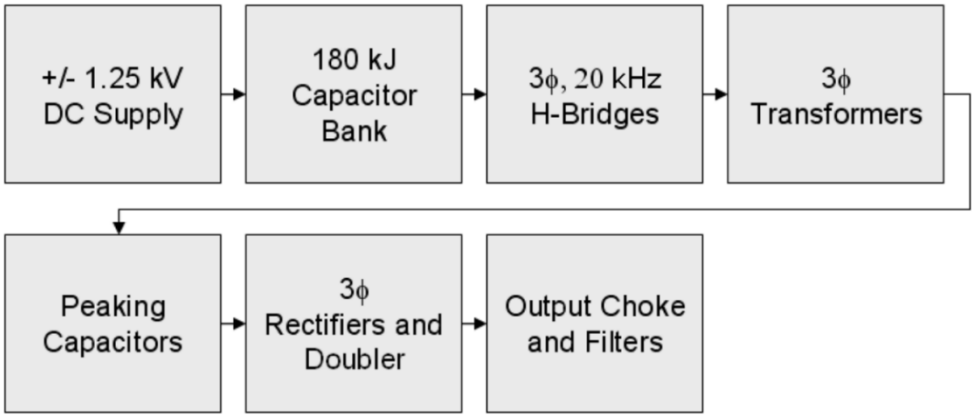
Resonant Converter-Modulator

- Switch-mode converter
  - Chopping at solid state switch voltage
  - AC transformer steps up to high voltage
  - High frequency inverter
    - Minimizes transformer size
    - Minimizes output filter size
    - Minimizes output pulse risetime
- Poly-phase for high power
- Resonant circuit
  - Transformer leakage inductance → high voltage
  - Tuning capacitor
- Rectification
- Filtering
  - Inductive
  - HF trap



Spallation Neutron Source: High Voltage Converter Modulator (HVCM)

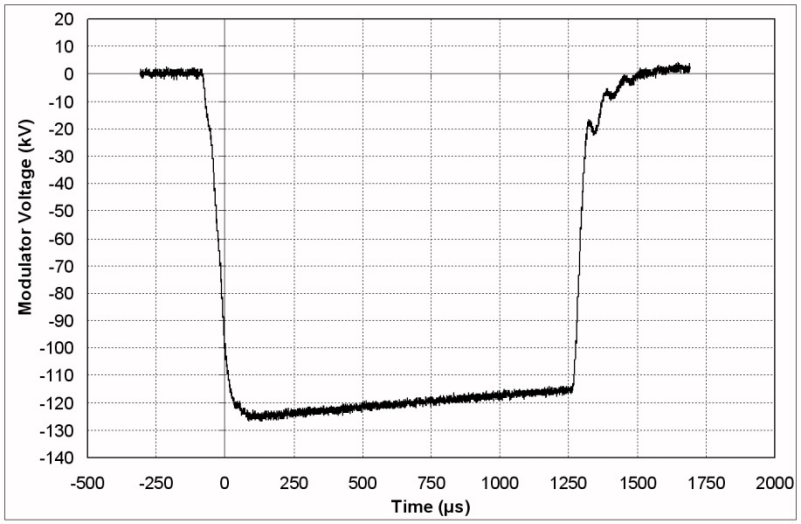
- Three-phase resonant converter modulator
- Primary power: ±1.25 kV
  - Compatible with HV IGBT modules
  - Air insulation, simplifies maintenance
- Resonant transformer
  - Inductance for switching circuit (zero-current switching)
  - Added voltage gain
  - Resonant circuit impedance tuned to load power needs
- 2X voltage multiplier after rectification
- Filtering to meet klystron regulation requirements
- Output
  - Average power: to 1 MW
  - Peak power: to 11 MW
  - Output voltage: 70 – 125 kV
  - Pulse length: 1.1 to 1.6 ms
  - PRF: to 60 Hz



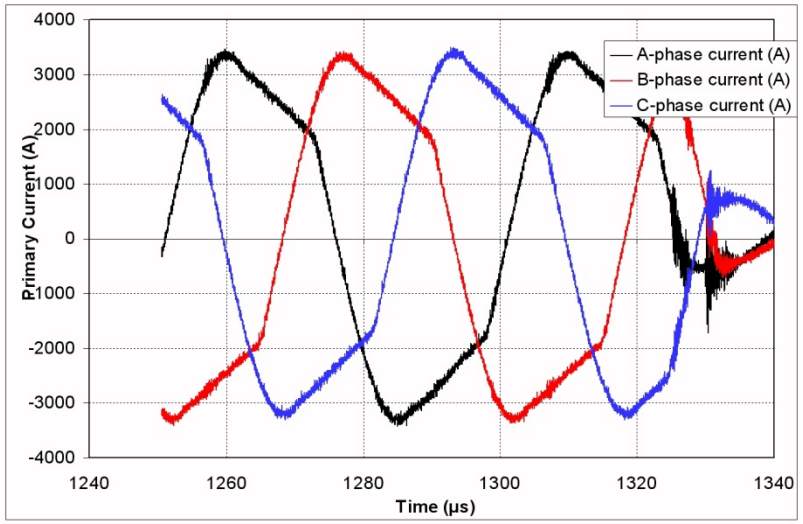
SNS HVCM

- 20 kHz inverter frequency
  - Small transformers
  - Small output filter
    - Fast risetime (~100 μs)
    - Low stored energy: minimize arc fault energy
- Low inverter voltage (~2 kV)
  - H-bridge is air insulated
  - Only low maintenance HV components are in oil
- The resonant peaking capacitors allow fault “ride-through” capabilities.
  - Load impedance changes (such as klystron discharges) de-tune the resonant circuit.
  - Down-side, resonant circuit tuning sensitive to changes in load (klystron perveance)
- Modulator was designed for PWM operation to obtain a well-regulated output pulse

SNS HVCM (Tuned for SLAC L-band)

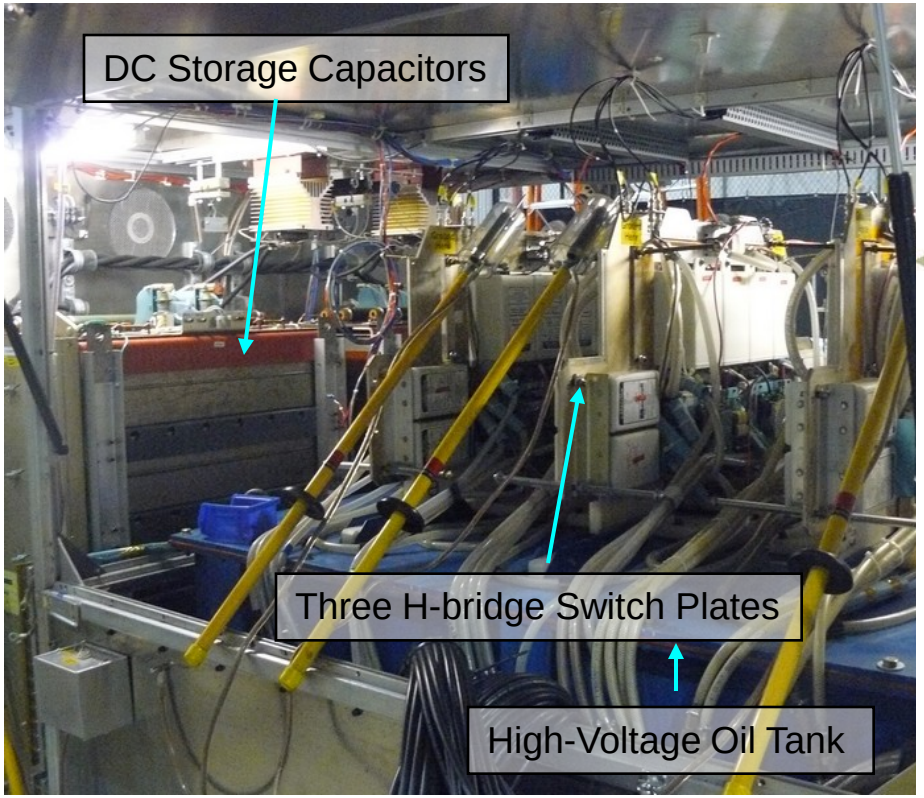


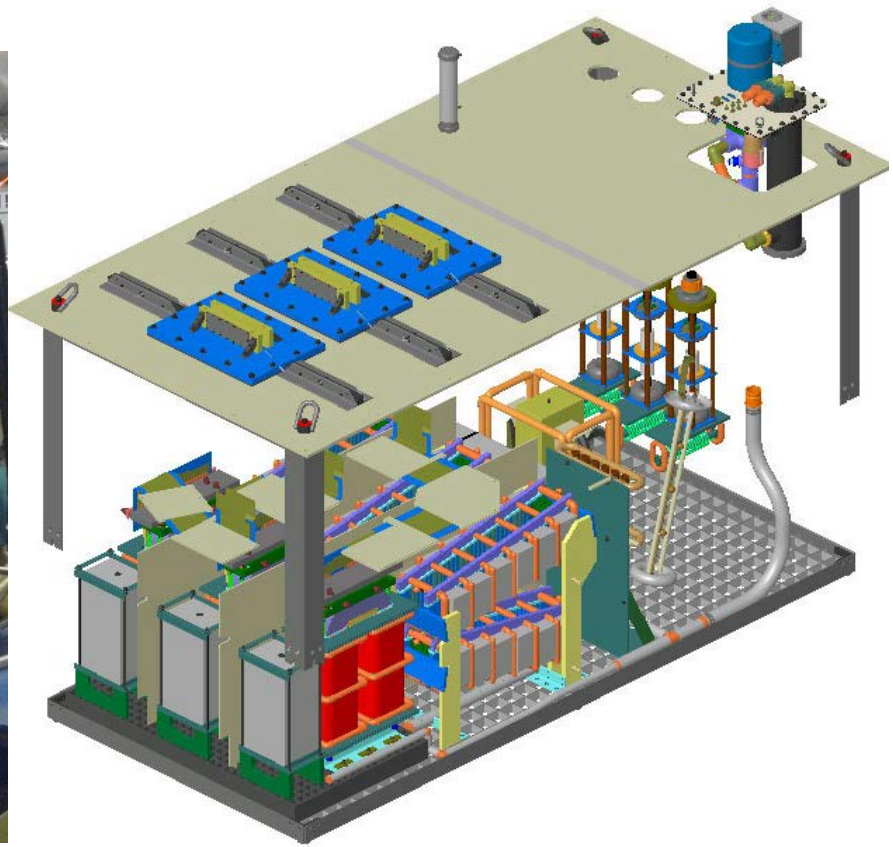
Output voltage waveform



Primary current waveforms

SNS HVCM





HV basket located inside oil tank

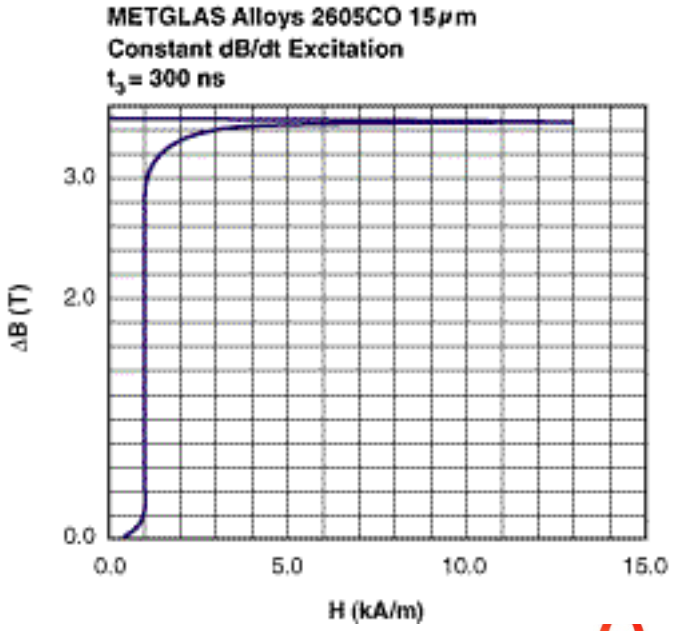
Magnetic Pulse Compression Circuits

- Magnetic Circuit/Systems
  - Basics
  - Relevant Equations
  - Limitations
  - Other Practical Consideration
  - Mechanical Design
  - Examples of Operational Systems
  - References

Magnetic Switch Principles

- A magnetic switch is a device, usually constructed as a winding around a magnetic core, that uses the non-linear properties of magnetic materials to achieve a large change in impedance
- The impedance of a magnetic switch varies from a large inductance (high permeability when magnetic core unsaturated) to a small inductance (low permeability when magnetic core saturated)

Note: With few exceptions a magnetic switch needs a “real” switch somewhere in the circuit ahead of the magnetic switch to initiate magnetic compression . This real switch will need to be capable of handling the same energy as the magnetic switch but at much lower peak power levels.

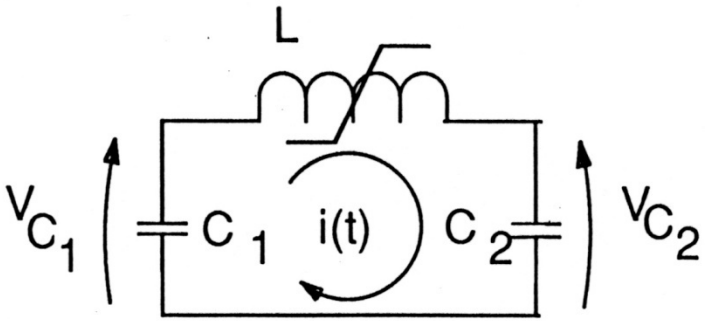


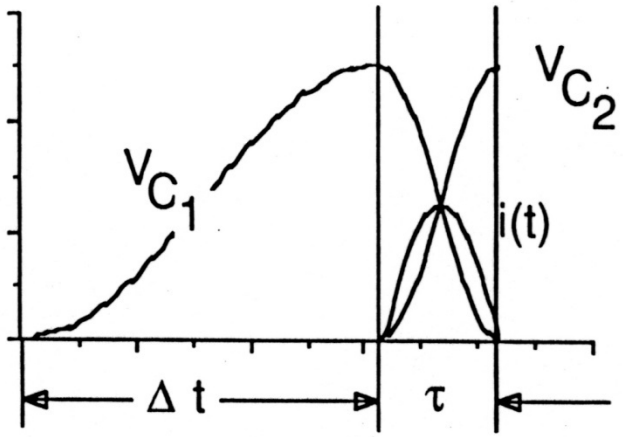
Definition of Terms

Term	Definition	Units
L_n	the n^{th} stage of magnetic compression	
Vol_n	minimum magnetic core volume of L_n	$meters^3$
A_n	magnetic cross-sectional area of L_n	$meters^2$
OD	outer diameter of magnetic core (toroid)	meters
ID	inner diameter of magnetic core (toroid)	meters
$^2 B_S$	usable change in core flux density	tesla
N_n	number of turns on the L_n winding	
w_n	axial length of L_n winding	meters
$^2 r$	radial thickness of magnetic core	meters
<r>	mean radius of magnetic core	meters
pf	packing factor - cross-section area of magnetic material divided by total area enclosed by windings	
L_n^{sat}	saturated inductance of L_n	henries
$Gain_n$	ratio of charge to discharge time for L_n	
C_n	capacitance at the input of L_n	farads
E_{Cn}	per pulse energy stored on C_n	joules
$<V_{Cn}>$	average charge voltage on capacitor C_n	volts
τ_{Cn}^{chg}	time required for capacitor C_n to charge to peak voltage	seconds
τ_{Ln}^{sat}	hold-off time - time required to saturate L_n at a given average charge voltage	seconds
t_{prop}	total propagation delay through the modulator - equal to the sum of the hold-off times of all the stages	seconds
μ_o	free space permeability = $4š*10^{-7}$	henries/m
μ_r	relative permeability	
μ_r^{sat}	saturated value of relative permeability	
$<\mu_r^{sat}>$	average relative permeability during saturation	
$^2 t$	time jitter	seconds
$^2 v$	pulse-to-pulse variations in peak charge voltage	volts

Magnetic Switch Operation

- **The Magnetic Switch is designed to saturate at the voltage peak on C_1 and transfer all the stored energy to C_2**



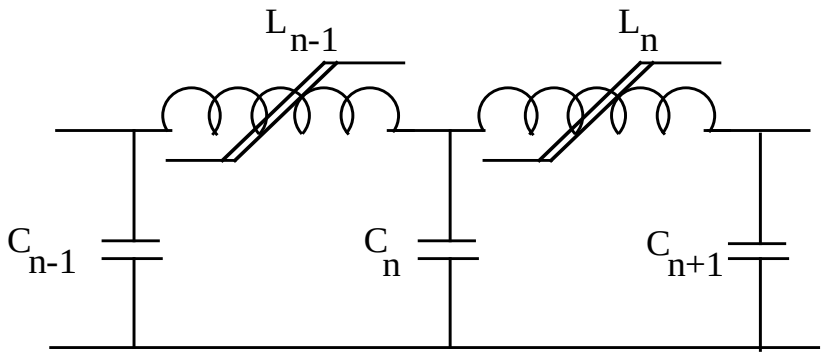


$$\text{GAIN} = \frac{\Delta t}{\tau}$$

Basic Compression Circuit Equations

$$\tau_{C_n}^{chg} = \pi\sqrt{L_{n-1}^{sat} C_{eq}} = \pi\sqrt{L_{n-1}^{sat}\frac{C_n}{2}} \qquad \textbf{(1)}$$

where: $C^{n-1} = C^{n} = C^{n+1}$



$$\tau_{C_n}^{chg} \approx \tau_{L_n^{sat}} = \frac{N_n A_n \Delta B_s}{< V_{C_n} >} \qquad \textbf{(2)}$$

The resonant charging voltage waveshape of this circuit has the form: And for this waveshape <V_{Cn}> is equal to Vpk/2 when integrated to the time of peak voltage.

$$V(t) = \frac{Vpk}{2}(1 - \cos(\omega t))$$

Combining the equations (1) and (2) and solving for L_{n-1}^{sat} gives:

$$L_{n-1}^{sat} = \frac{\left(\frac{2N_n A_n \Delta B_s}{\pi}\right)^2}{\frac{1}{2} C_n V_{pk}^2} = \frac{\left(\frac{2N_n A_n \Delta B_s}{\pi}\right)^2}{E_{C_n}} \qquad \textbf{(3)}$$

Where E_{Cn} is the peak energy stored in C_n

Basic Compression Circuit Equations

- The previous equations define switch parameters as functions of circuit values and magnetic material properties. Into these equations we need to incorporate equations defining switch geometry.

- The inductance of a toroid of rectangular cross section is given by:

$$L = \frac{1}{2\pi}\mu_r \mu_o w N^2 \ln\left(\frac{OD}{ID}\right) \qquad \textbf{(4)}$$

- Substituting the saturated value of L_n into this equation gives:

$$L_n^{sat} = \frac{1}{2\pi}\mu_r^{sat} \mu_o w_n N_n^2 \ln\left(\frac{OD}{ID}\right) \qquad \textbf{(5)}$$

- Dividing this into the relation for $L_{n-1}{}^{sat}$ (Eq. (3))yields:

$$\frac{L_{n-1}^{sat}}{L_n^{sat}} = \frac{2\Delta B_s^2 A_n^2}{10^{-7}\pi^2 \mu_r^{sat} w_n \ln\left(\frac{OD}{ID}\right) E_{C_n}} \qquad \textbf{(6)}$$

Basic Compression Circuit Equations

- However:

$$\frac{L_{n-1}^{sat}}{L_n^{sat}} = \left(\frac{\tau_{C_n}^{chg}}{\tau_{C_{n+1}}^{chg}} \right)^2 = Gain_n^2 \qquad (7)$$

- and therefore:

$$Gain_n^2 = \frac{2\Delta B_s^2 A_n^2}{10^{-7}\pi^2 \mu_r^{sat} w_n \, ln\left(\frac{OD}{ID}\right) E_{C_n}} \qquad (8)$$

- Using the expansion for the natural log term:

  $w \ln(OD/ID) \approx w\,\Delta r/\langle r\rangle = A_n/\langle r\rangle$

$$L_n^{sat} \approx \frac{\mu_r^{sat}\mu_o N_n^2 A_n}{2\pi \langle r \rangle} = \frac{\mu_r^{sat}\mu_o N_n^2 A_n^2}{Vol_n} \qquad (9)$$

- Dividing eq. (3) by (9) and rearranging gives:

$$Vol_n \approx \frac{Gain_n^2 E_{C_n} \pi^2 \mu_r^{sat} \mu_o}{4\Delta B_s^2} \qquad (10)$$

Basic Compression Circuit Equations

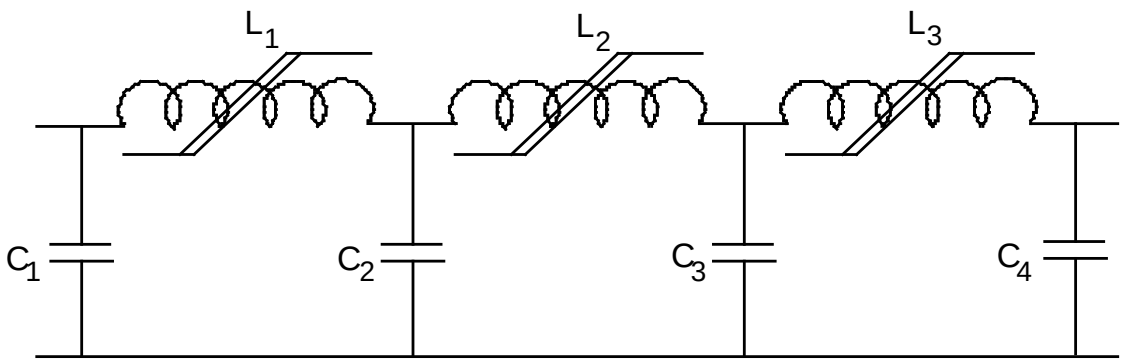
- Vol_n in Eq. (10) represents the minimum volume of magnetic material (and therefore minimum loss) required for a switch, L_n, given a required gain, per pulse energy, and ΔB_s. Eq. (10) assumes that the entire toroidal volume inside the winding is filled with magnetic material. This is never achieved in practice and the term packing factor (pf) is defined:

  pf = the cross-section area of magnetic material divided by the total area enclosed by the windings

  This modifies the minimum volume equation to the following:

$$Vol_n \approx \frac{Gain_n^2 E_{C_n} \pi^2 \mu_r^{sat} \mu_o}{\mathrm{pf} 4 \Delta B_s^2}$$

Magnetic Compression Circuits



- To achieve higher overall gain, multiple switches may be used
  - Switches are designed to saturate sequentially
  - Multiplying individual switch gains yields the overall gain
- Capabilities of magnetic compression systems
  - High repetition rate
  - High average power
  - Very high peak power
  - High reliability
- Note: A “real” switch (one than can be controlled by external trigger is required to initiate the magnetic compression sequence

Magnetic System Limitations- Jitter

- Time Jitter - caused by variations of voltage and ΔB as per:

$$\tau_{C_n}^{chg} \approx \tau_{L_n^{sat}} = \frac{N_n A_n \Delta B_s}{< V_{C_n} >}$$

  - Jitter is proportional to the total propagation delay through the magnetic system (sum of the individual switch hold-off times)
    - Example: If the total propagation delay is 10μs and the average input voltage variation is 1% the minimum time jitter (ΔB variation is zero) is:
      - $\Delta t \sim 10\mu s * .01 = 100ns$
  - Jitter can be minimized by:
    - Precisely resetting the magnetic cores prior to the next pulse
    - Precise voltage regulation or real-time adjustment of trigger pulse to compensate for ΔV
- Jitter of < ± 2ns can be reasonably anticipated for systems having propagation delays < 10 μs

Magnetic System Limitations - Risetime & Repetition Rate

- Risetime: the pulse risetime is determined by the saturated inductance of the winding geometry. It is possible to obtain single turn inductance in the nH range. In practice, output risetimes in the range of 10-20 ns are routinely achieved for high voltage systems

- Repetition Rates:
  - Burst Repetition Rate
    - Parallel systems (Branch Magnetics) can operate at 10's of MHz
    - Single pass systems can probably work up to ~ 100 kHz (the limitation is that all the magnetic cores need to be reset between pulses
  - Constant Repetition Rate
    - Single pass systems can operate into the 10-20 kHz region (liquid cooling is required to remove heat generated in the magnetic cores and capacitors)
      - Metglas™ is limited to < 5 kHz for the fastest saturation rates (output stages) but may easily be used for earlier stages. Another limitation of Metglas™ at fast saturation rates (high $\Delta B/\Delta t$) is voltage breakdown between laminations
      - Ferrites are often used for the output stages in high rep-rate systems

Magnetic System Limitations - Number of Stages

- The total gain required by the system determines the number of stages where the total gain in the product of the individual switch gains
  - Individual switch gain is restricted by the core volume relationship:

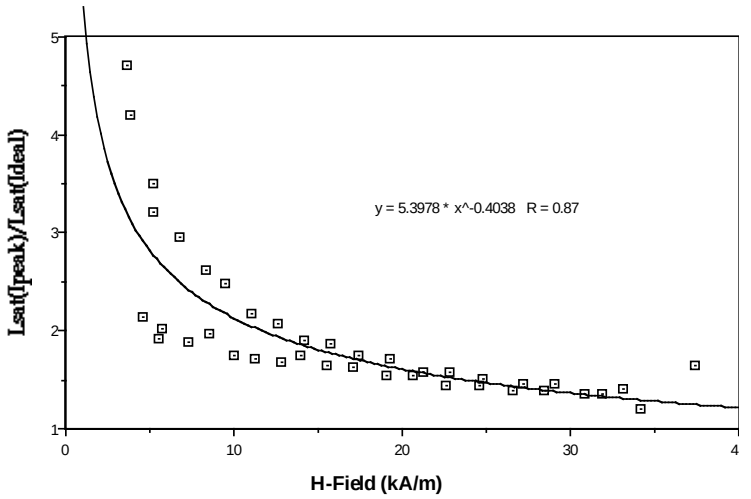
$$Vol_n \approx \frac{Gain_n^2 E_{C_n} \pi^2 \mu_r^{sat} \mu_o}{4 \Delta B_s^2}$$

    - Maximum reasonable core gain:
      - ~ 3 for ferrite
      - 5-10 for Metglas™ and other amorphous materials
- When more than two switches are required, a step-up transformer is normally needed (eliminates trying to design fractional turn switches)
- Usually only 3 magnetic switches are required to cover the range of microseconds (initial conduction time) to nanoseconds (output risetime)

Other Practical Considerations - μ_r^{sat}

- Saturated permeability - The assumption is that the saturated inductance of a magnetic switch may be calculated by assuming that μ_r has the value of unity (free space). While this is a valid assumption when the H field is high enough, empirical data indicated that surprisingly large values of ampere turns are required to fully saturate a magnetic core. The net effect is that during the time of saturation and energy transfer through the magnetic switch the average value of saturated permeability should be considered as having a value somewhere between 1 and 2. The actual value will be dependent on the magnetic core material chosen and the geometry of the winding around the core.

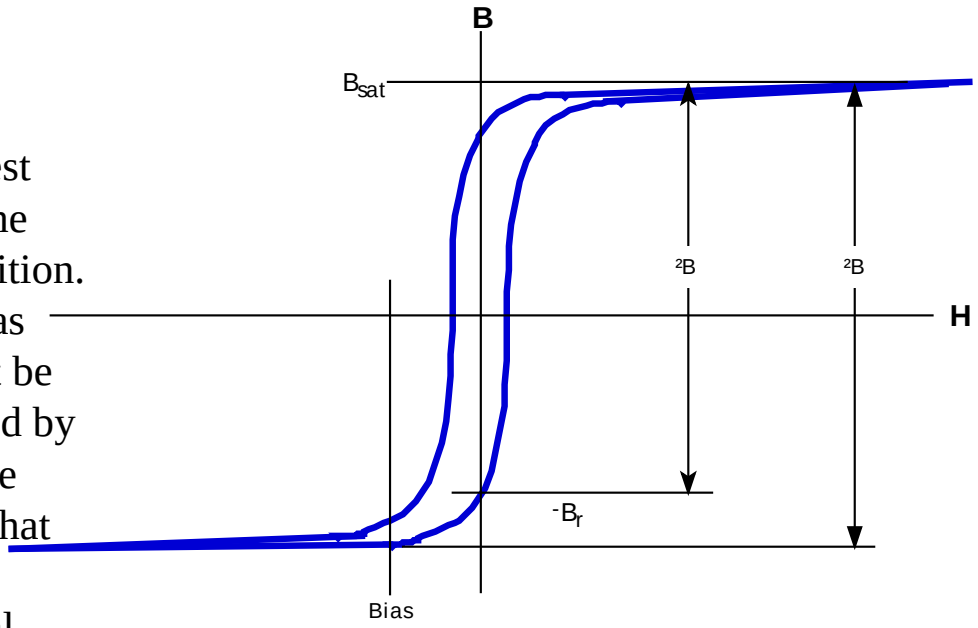
This curve is generated by allowing a magnetic switch to ring in a resonant, low loss circuit. The average saturated inductance (calculated from the peak current of the oscillations) is divided the calculated air core inductance for $\mu_r = 1$ and plotted versus the peak H-field corresponding to each value of peak current. Note that the inductance ratio levels out at ~ 1.5 for a peak field of~ 25kA/m: this indicates that the core is fully saturated and that the winding geometry is responsible for the measured inductance being higher than the calculated value.



Ratio of Inductance Values versus Peak H-Field (Ferrite Core)

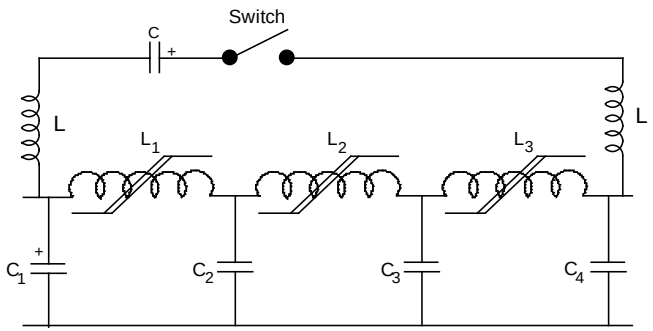
Other Practical Considerations - Reset/Bias

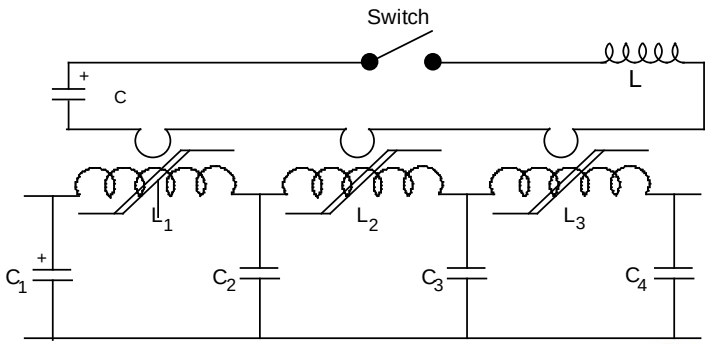
Reset/Bias - Achieving consistent performance from a magnetic switch requires that the initial state of the magnetic core be known and the easiest way to know the initial condition of the magnetic is to force it to a known position. This is usually the task of the reset/bias circuit. The magnetic cores must first be reset - in essence the volt-seconds used by the switch must be replaced by voltage applied of the opposite polarity such that the volt-second product is equal to or greater than that used during the initial energy compression. The cores can be reset by voltage applied to the main windings or to a turn through the core that is not part of the pulse power circuit (in essence a secondary winding as the magnetic switch will function as a transformer until the core material is again saturated). In either case the reset circuit must be protected/isolated from the high-voltage pulses generated during normal operation. Isolation is usually achieved by using large inductors although diode isolation can be used. DC bias is used to hold the magnetic core at a particular point on the BH curve and provides the additional benefit of increasing the useable ΔB for a given core. Note the polarity of the bias current is opposite the switch discharge current.



Other Practical Considerations - Reset/Bias Circuits.

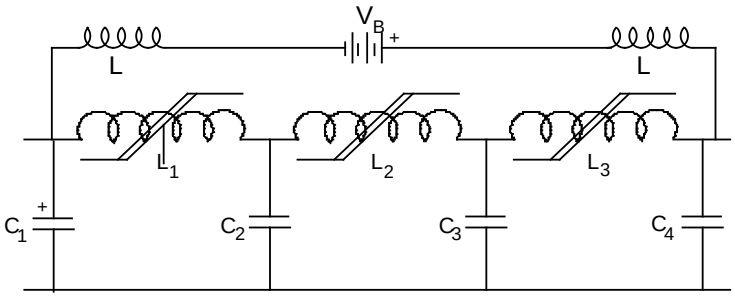
- Two different type of reset circuits can be used -
  - Pulsed reset: a voltage pulse (usually having an amplitude substantially less that the operation voltage) is applied to the core
    - Advantages:
      - fast: the core can be reset quickly if needed for high repetition rates.
      - efficiency: only the energy needed to reset the core is required
      - increased ΔB: the core can be driven all the way to $-B_{sat}$
    - Disadvantages:
      - complexity: requires a switch, extra capacitors, power supply, and a properly timed trigger signal
      - circuit cannot be allowed to ring or the magnetic switch must operate while the reset pulse is on (still at $-B_{sat}$)

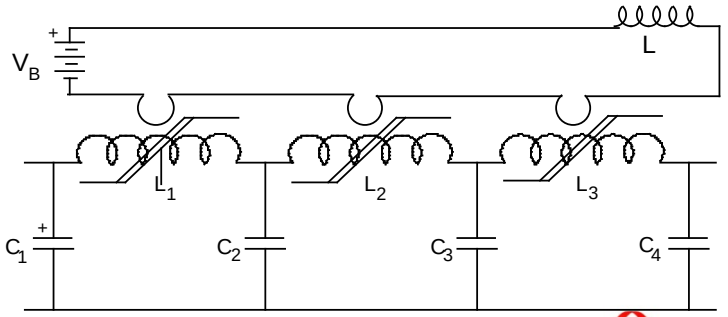




Other Practical Considerations - Reset/Bias Circuits

- DC reset: a low voltage DC power supply is connected to the magnetic switch through an large inductor (compared to the pulse duration) thereby creating a current source
  - Advantages:
    - simplicity: few components and no timing requirements
    - inexpensive: components not costly
    - reliability: not much to break
    - Increased ΔB: the DC reset also serves as a DC bias
  - Disadvantages:
    - efficiency: the power supply is usually on all the time





Mechanical Design

- The mechanical design of a magnetic switch is more complicated than the electrical portion of the design.
- The mechanical is guided by two contradictory requirements:
  - the need to minimize inductance of the winding structure (including connections to capacitors and other switches) in order to optimize the performance of the magnetic switch
  - the need to ensure reliable performance of a winding structure that must operate at high voltage
- In addition, the mechanical design must have sufficient mechanical robustness to adequately support the magnetic material (which may have substantial weight) and ensure that the position of the windings is controlled and the inductance of the mechanical structure is fixed and repeatable (particularly if production quantities are envisioned).
  - In general, turns of wire around a core are not going to meet these requirements.

Mechanical Design

- A common method of constructing a magnetic switch on a toroidal core of rectangular cross-section is to use metal rods on the inside diameter (ID) and outside diameter (OD). Crossover links on the ends of the switch may be fabricated with metal bars or may be attached to a printed circuit board.
  - For calculation of the inductance use the dimensions to the middle of the rods (for ID and OD)
  - When only a few turns are needed, use multiple sets of windings to enclose the core as completely as possible.
  - When using nickel-zinc ferrite (high intrinsic resistance),the turns can be touching the core
  - Connections between the magnetic switch and capacitors should be as short and wide (such as a parallel plate layout) as possible to minimize inductance
  - The spacing between conductors at high voltage should be adequate to prevent electrical breakdown and all edges of high voltage conductors should have as large a radius as possible in order to reduce field enhancement

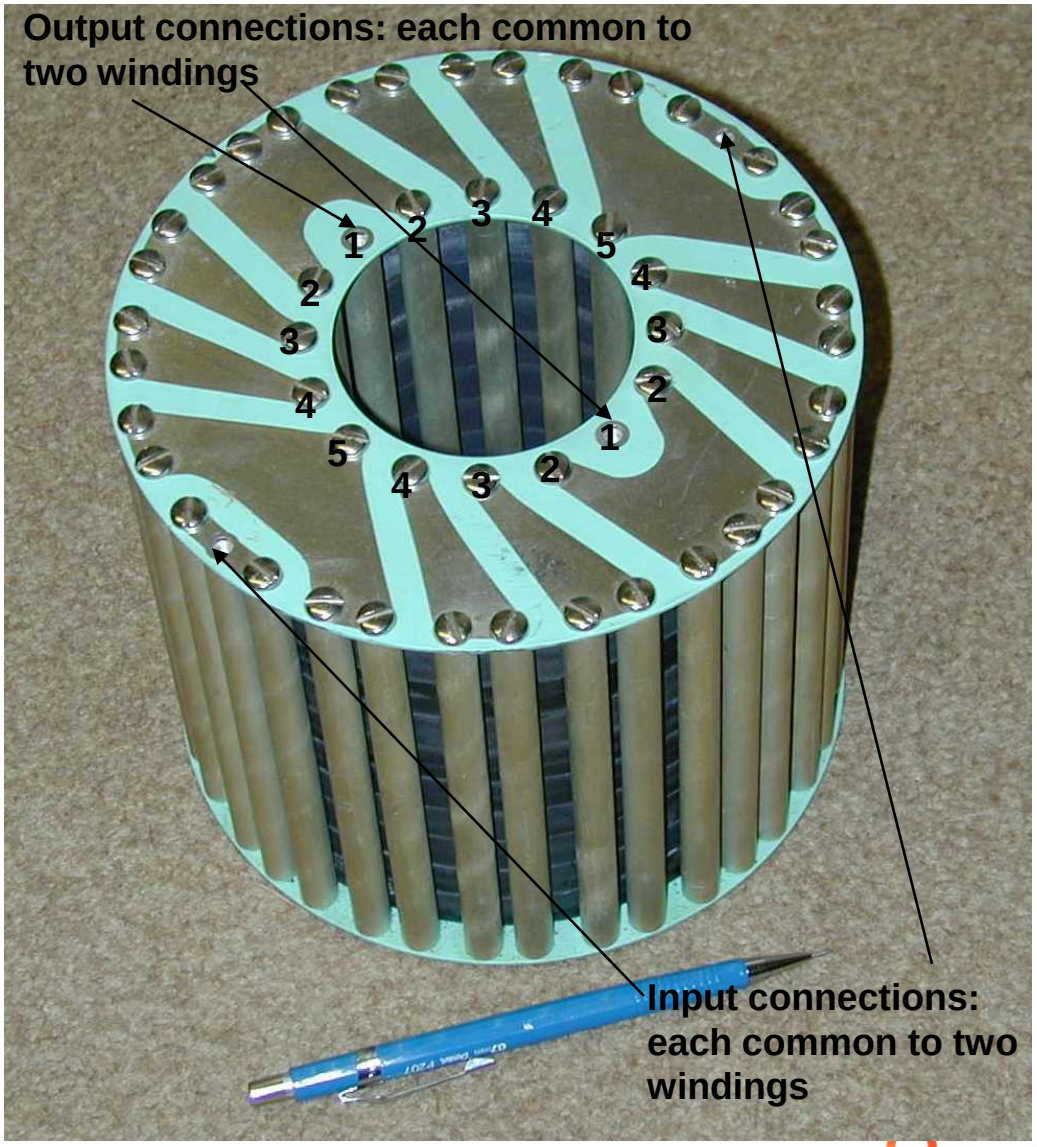
Mechanical Design - Example

5 -Turn Switch
(configured as 4 sets of 5 turns)

20kV hold-off for 1μs with gain of 3.0 using ferrite toroids.

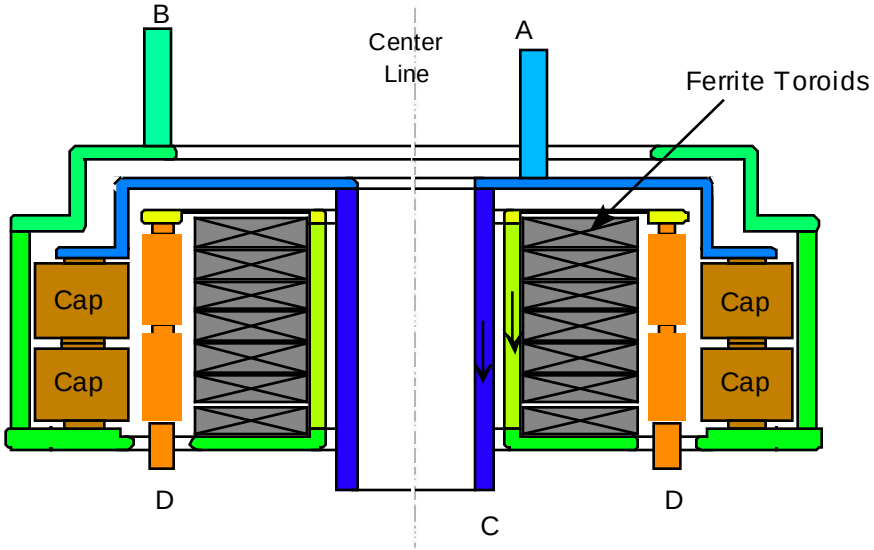
Inside and outside turns are fabricated of 0.375” Dia. rod.

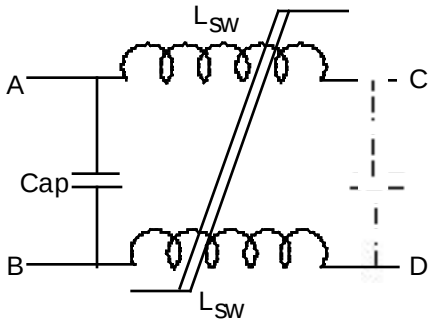
Crossover connections between inside and outside rods are patterns on printed circuit boards. Board pattern on top and bottom boards are different.



Mechanical Design - Example

- When only one or two turns are required, tubes and concentric tubes can be used as the turns through the center of the core
  - Remember that the current return on the outside of the core needs to close to the core to minimize the inductance



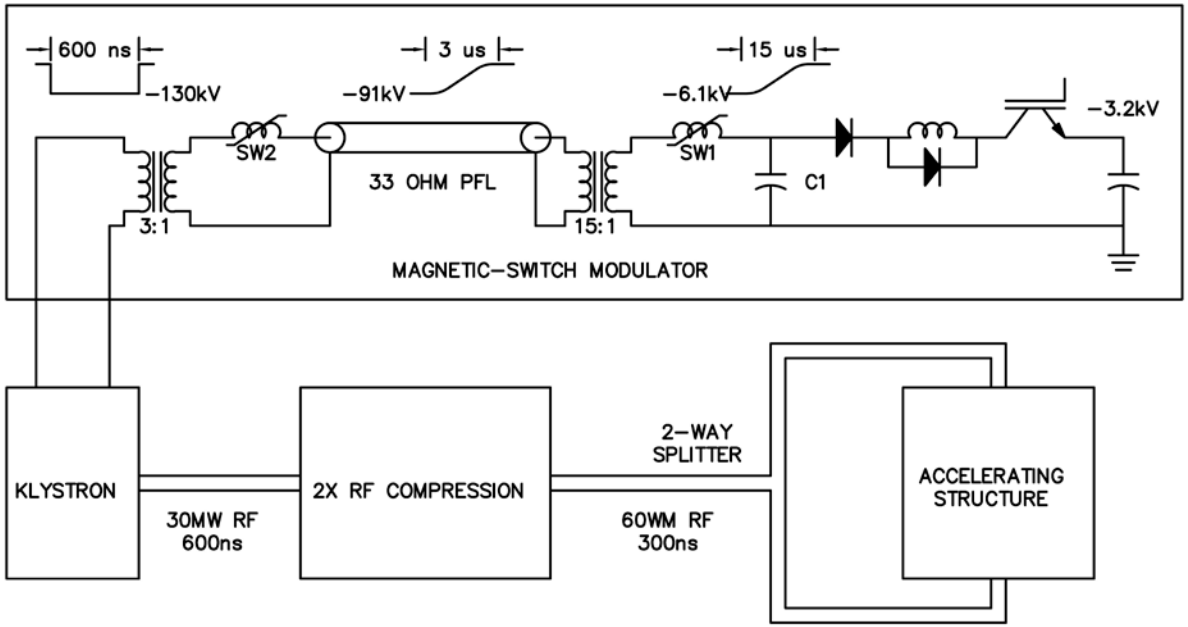


Electrical Schematic

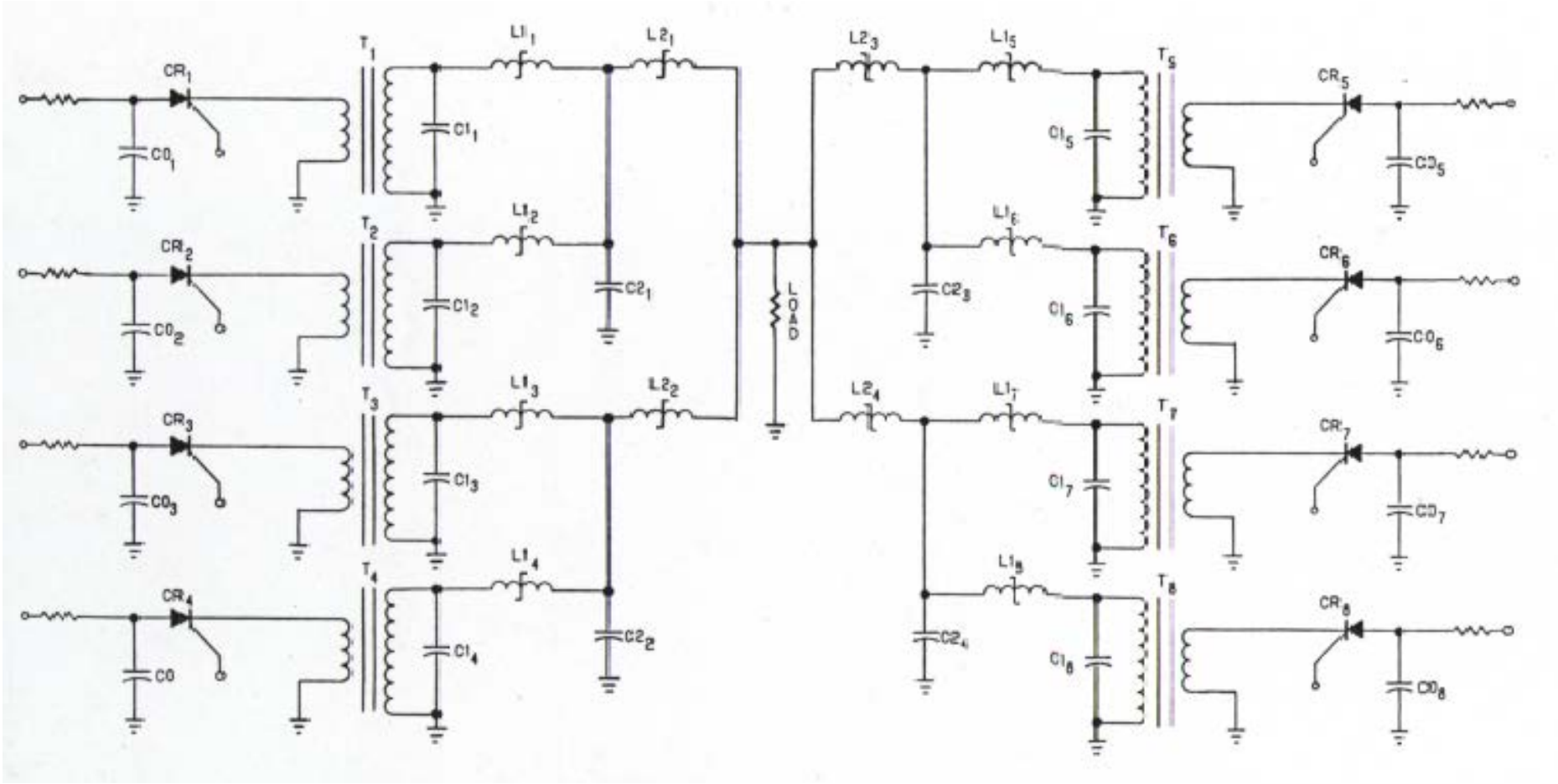
Cross-section of 2-turn magnetic switch with turns split as shown in the schematic. This approach is used to reduce maximum field stress to ground by operating at positive and negative input voltages with respect to ground.

Conceptual X-Band Klystron Magnetic Modulator

- IGBT module for 1st stage switching
- 1st magnetic switch charges water PFL through HV pulse transformer
- 2nd magnetic switch discharges PFL through pulse transformer to match klystron impedance
- Very high perveance, X-band MBK load
- Short modulator pulse minimizes Rf pulse compression costs/losses

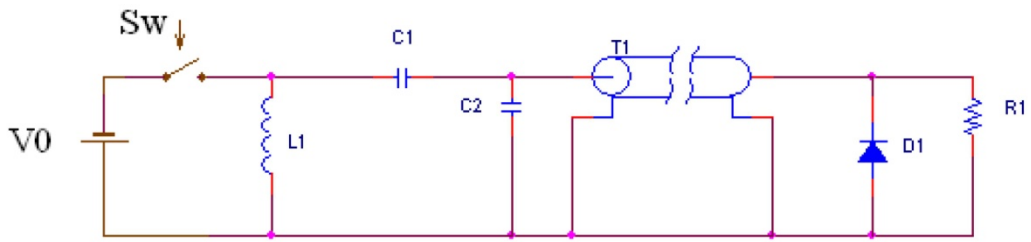


8-Pulse Demonstration Generator [Branch Magnetics]
35MHz - Maximum Burst Frequency



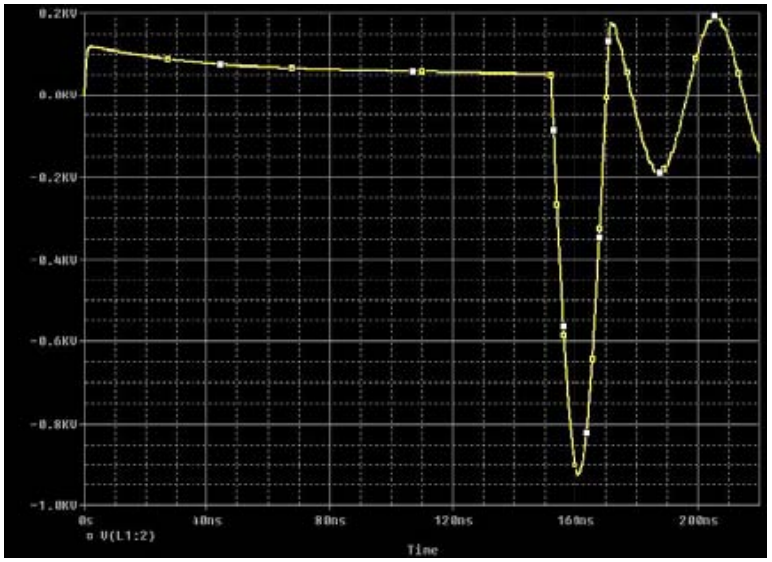
Firing Sequence - CR1, CR3, CR5, CR7, CR2, CR4, CR6, AND CR8

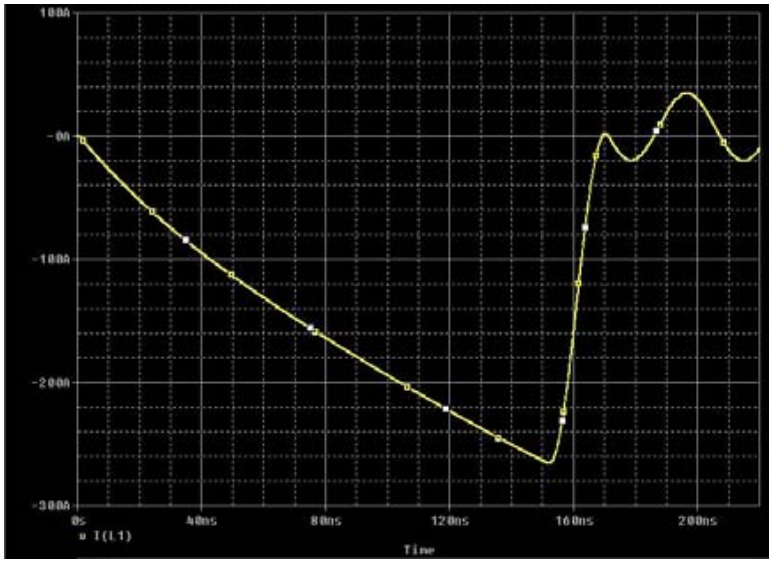
Ultra-fast DSRD Switched TL Modulator



- DSRD as a sub-ns opening switch for a transmission line modulator for the ILC damping ring kickers
  - 5 kV into 50 Ω
  - 4 ns flattop, <1 ns rise/fall (simulations for 2 ns pulse)
  - Bunch separation <10 ns
  - 3 (or 6) MHz burst at 5 Hz
- Switch, SW, is closed to charge L1, some parasitic component is transferred through C1/T1 for forward bias D1
- SW opens, L1 discharges into T1 via C1 (resonant transfer), D1 is still in conduction (reverse recovery charge), shorting T1 (current charging of T1 inductance)
- Energy transfer from L1 to T1 is completed as D1 opens
- T1 now connected to matched load, R1

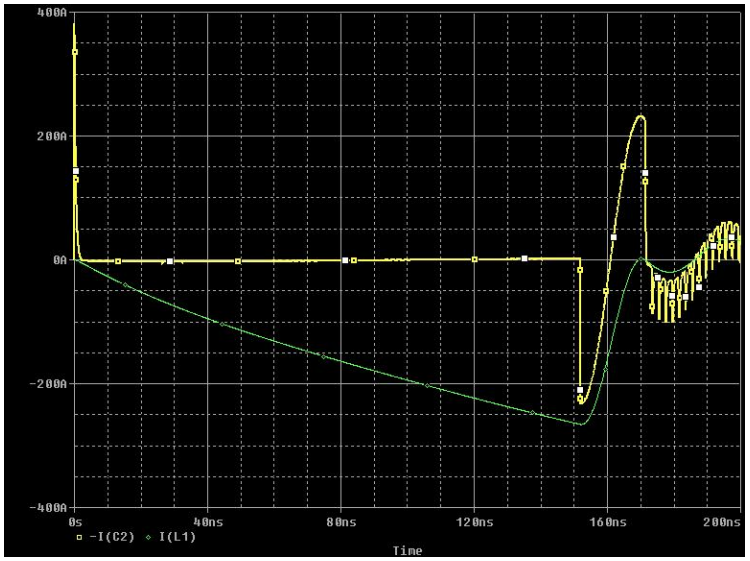
DSRD Modulator Energy Transfer Sequence



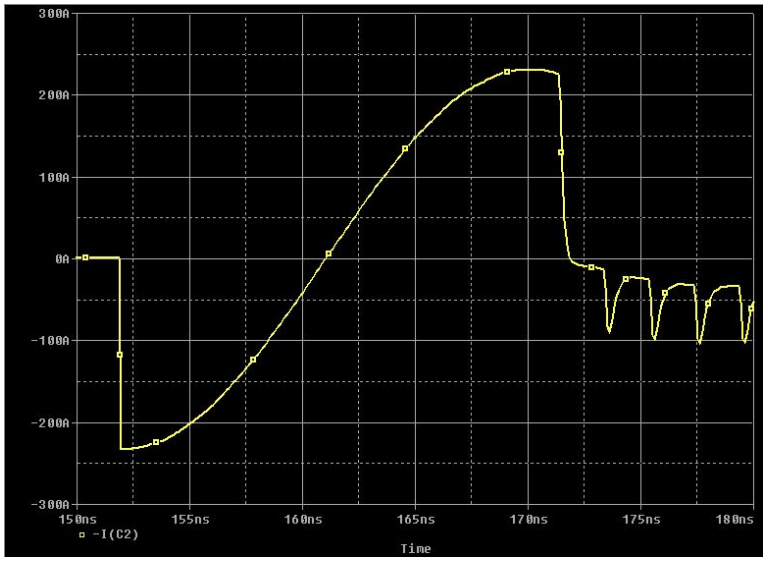


- Voltage (left) and current of L1 during charging period (SW closed)

DSRD Modulator Energy Transfer Sequence (cont)



(a)



(b)

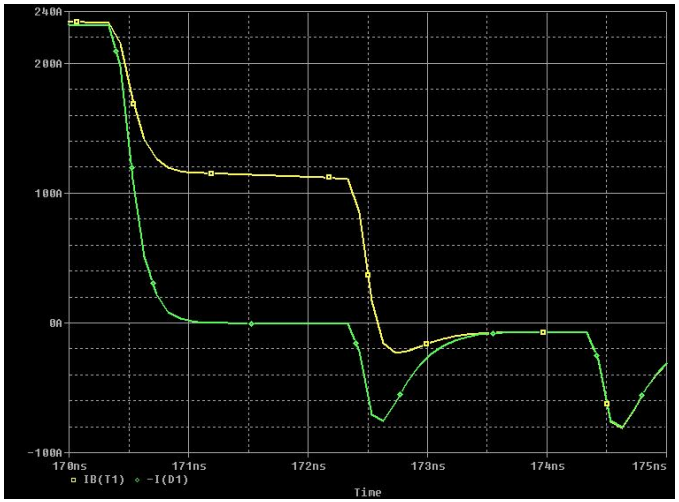
(a): Current in L1 (green) and C2 (yellow) during charging of L1 (t<154 ns) and transfer to T1

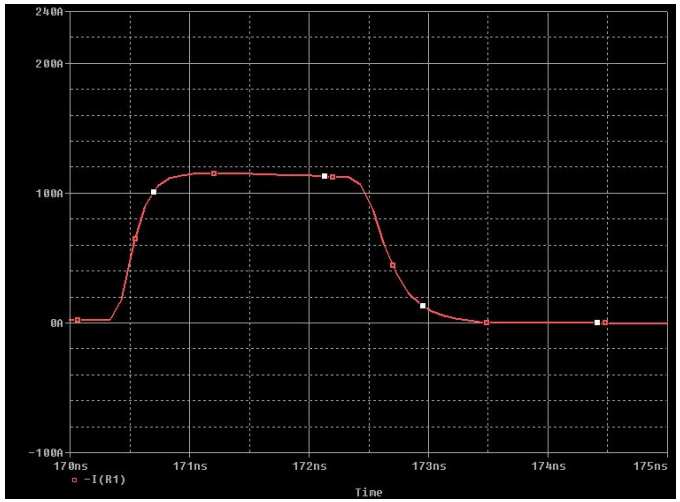
(b): Detail of C2 current during energy transfer to T1 (t<170.5 ns) and discharge into load, note current through C2 until halfway through T2 discharge (t=171.5 ns)

(c): D1 current (green) and T1 current, load end, (yellow)

(c)

DSRD Modulator Energy Transfer Sequence (cont)





- Detail of D1 current (green) and T1 current, load end, (yellow) during transfer of energy to load (above right)
- Load current during discharge of T1 (above left)
- Challenges
  - Pre-pulse: finite DSRD turn-on time and forward-voltage
  - Post-pulse: residual energy will “bounce around” and come out at later time
  - Optimum timing dependent on precise DSRD properties that depend are temperature dependent